

Proposal to provide command integrity checking

Pete McLean
 Maxtor Corporation
 2452 Clover Basin Drive, CO 80503
 303 678-2149
pete_mclean@maxtor.com

18 January 2002

Transaction integrity becomes more important for ATA devices every year. In the words of Hale Landis, "Current ATA provides less integrity than computer systems of twenty years ago." This needs to be fixed.

With the introduction of CRC on Ultra DMA, errors in the transfer of user data are now detected. However, errors in the transfer of commands and command parameters are still not detected. Therefore, it is possible to read or write the wrong data on the disk or in some cases execute the wrong command.

It is the intent of this proposal to provide an optional error detection mechanism on commands and command parameters for 48-bit Address feature set [commands plus selected additional non-48-bit Address feature set commands](#).

Add new clause:

6.x Command Consistency feature set

The Command Consistency feature set is an optional feature that may be used with devices that implement the 48-bit Address feature set. It provides error detection on the delivery of commands and the parameters associated with the commands.

[The Command Consistency feature set, when enabled, shall apply to the following commands:](#)

- [DOWNLOAD MICROCODE](#)
- [FLUSH CACHE EXT](#)
- [IDENTIFY DEVICE](#)
- [READ DMA EXT](#)
- [READ DMA QUEUED EXT](#)
- [READ MULTIPLE EXT](#)
- [READ NATIVE MAX ADDRESS EXT](#)
- [READ SECTOR\(S\) EXT](#)
- [READ VERIFY SECTOR\(S\) EXT](#)
- [SECURITY SET PASSWORD](#)
- [SERVICE](#)
- [SET MAX ADDRESS](#)
- [SET MAX ADDRESS EXT](#)
- [SLEEP](#)
- [SMART](#)
- [STANDBY](#)
- [WRITE DMA EXT](#)
- [WRITE DMA QUEUED EXT](#)
- [WRITE MULTIPLE EXT](#)
- [WRITE SECTOR\(S\) EXT](#)

The Command Consistency feature set may be enabled via a SET FEATURES command with subcommand value TBD and may be disabled via a SET FEATURES command with a subcommand value of TBD. Support for the Command Consistency feature set shall be indicated by bit TBD of word 84 and bit TBD of word 87 shall indicate when the feature is enabled.

When the Command Consistency feature set is supported and enabled, the Device/Head register becomes a 16-bit register just like the Sector Count, Sector Number_LBA Low, Cylinder_High_LBA Mid, and Cylinder_Low_LBA High registers with the 48-bit Address feature set commands. The value that was in the Device/Head register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte.

When issuing a 48-bit Address Command Consistency feature set commands with Command Consistency enabled, the host shall write the content of all registers as described in the command description except the Device/Head register. The Device/Head register shall be written with the Command Consistency value that is calculated as follows and as shown in figure xx:

Features_Ext is defined as a 16-bit value where the value that was in the Features register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte. For commands that do not use the value that was in the register before the most recent write, the high order byte shall set to a value of zero.

Sector_Count_Ext is defined as a 16-bit value where the value that was in the Sector Count register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte. For commands that do not use the value that was in the register before the most recent write, the high order byte shall set to a value of zero.

Sector_Number_LBA Low_Ext is defined as a 16-bit value where the value that was in the Sector Number_LBA Low register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte. For commands that do not use the value that was in the register before the most recent write, the high order byte shall set to a value of zero.

Cylinder_Low_LBA Mid_Ext is defined as a 16-bit value where the value that was in the Cylinder Low_LBA Mid register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte. For commands that do not use the value that was in the register before the most recent write, the high order byte shall set to a value of zero.

Cylinder_LBA High_Ext is defined as a 16-bit value where the value that was in the Cylinder_LBA High register before the most recent write to the register is the high order byte of the 16-bit value and the most recently written value is the low order byte. For commands that do not use the value that was in the register before the most recent write, the high order byte shall set to a value of zero.

Command_Ext is defined as a 16-bit value where the low order byte is the value most recently written to the Command register and the value if the high order byte is 00h.

The Command Consistency value (CCV) is the value written to the Device/Head register.

- a) The Command Consistency value 1 (CCV1) is set equal to Features_Ext.
- b) CCV1 is rotated left one bit and then Sector_Count_Ext is Exclusive ORed into CCV1.

- c) CCV1 is rotated left one bit and then Sector_NumberLBA_Low_Ext is Exclusive ORed into CCV1.
- d) CCV1 is rotated left one bit and then Cylinder_LowLBA_Mid_Ext is Exclusive ORed into CCV1.
- e) CCV1 is rotated left one bit and then CylinderLBA_High_Ext is Exclusive ORed into CCV1.
- f) CCV1 is rotated left one bit and then Command_Ext is Exclusive ORed into CCV1.
- g) CCV2 is set equal to CCV1 ANDed with the value 5050h.
- h) CCV2 is shifted left one bit.
- i) CCV is set equal to CCV1 Exclusive ORed with CCV2.
- j) If the command is being sent to Device 0, the value EFEFh is ANDed in CCV, then the value 4040h is ORed into CCV, and the result is written to the Device/Head register.
- k) If the command is being sent to Device 1, the value 5050h is ORed into CCV, and the result is written to the Device/Head register.

The Command Consistency values written to the Device/Head register using this algorithm always result in the proper value being written into the DEV bit, bit 4, and the LBA bit, bit 6.

1)	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	Features_Ext
2)	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	1) rotated left
3)	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	Sector_Count_Ext
4)	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	2) ⊕ 3)
5)	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	4) rotated left
6)	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	Sector_NumberLBA_Low_Ext
7)	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	5) ⊕ 6)
8)	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	7) rotated left
9)	f	f	f	f	f	f	f	f	f	f	f	f	f	f	f	Cylinder_LowLBA_Mid_Ext
10)	g	g	g	g	g	g	g	g	g	g	g	g	g	g	g	8) ⊕ 9)
11)	g	g	g	g	g	g	g	g	g	g	g	g	g	g	g	10) rotated left
12)	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	CylinderLBA_High_Ext
13)	j	j	j	j	j	j	j	j	j	j	j	j	j	j	j	11) ⊕ 12)
14)	j	j	j	j	j	j	j	j	j	j	j	j	j	j	j	13) rotated left
15)	k	k	k	k	k	k	k	k	k	k	k	k	k	k	k	Command_Ext
16)	l	l	l	l	l	l	l	l	l	l	l	l	l	l	l	14) ⊕ 15)
17)	0	l	0	l	0	0	0	0	l	0	l	0	0	0	0	16) ANDed with 5050h
18)	l	0	l	0	0	0	0	l	0	l	0	0	0	0	0	17) shifted left
19)	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	16) ⊕ 18)
If Device 0																
20)	m	m	m	0	m	m	m	m	m	m	0	m	m	m	m	19) ANDed with EFEFh
21)	m	1	m	0	m	m	m	m	m	1	m	0	m	m	m	20) ORed with 4040h
Value 21) is written to the Device/Head register																
If Device 1																
22)	m	1	m	1	m	m	m	m	1	m	1	m	m	m	m	19) ORed with 5050h
Value 22) is written to the Device/Head register																

Figure xx – Command Consistency value calculation

When the eCommand register is written with a [48-bit Address-Command Consistency](#) feature set command, the device shall calculate the Command Consistency value just as the value was calculated by the host and the device then compares the calculated value with the value in the Device/Head register. If the values match, the command is executed normally. If the values do not match, the device does not execute the command and returns ending status with the ICRC and ABRT bits set to one in the Error register.

8.xx.4 Inputs

In the input clause of each [48-bit Address-Command Consistency](#) feature set command add reference to the optional 16-bit Device/Head register.

8.14 IDENTIFY DEVICE

Table 24 words 84 and 87 add:

84		n	1 = Command Consistency feature set supported
87		n	1 = Command Consistency feature set enabled

8.45 SET FEATURES

Table 32 add:

nnh	Enable Command Consistency feature set
nnh	Disable Command Consistency feature set

Add 8.45.xx Enable/disable Command Consistency feature set

Subcommand code nnh allows the host to enable the Command Consistency feature. Subcommand code nnh allows the host to disable the Command Consistency feature.