

Accredited Standards Committee*
NCITS, National Committee for Information Technology Standards

Doc. No.: T13/E02001R0
 Date: 1/21/2002
 Project: 1484D
 Ref. Doc.: E01035R0
 D1484R2
 Reply to: Peter McLean

To: Membership of T13

Subject: Results of letter ballot E01035R0

For the ballot to forward Draft Standard 1484D, EDD – 2 revision 2, to NCITS for further processing, the vote was as follows:

When the ballot was issued on 17 December 2001, twenty-one voting member organizations existed. The results of the letter ballot are 17 yes votes, 0 no votes, 0 abstain votes, 4 eligible organizations did not vote. The motion passes. Details of the vote appear below.

Phil Gardner	Absolute Software	P	Yes
Ron Roberts	Adaptec	P	Yes
Larry Barras	Apple	P	Yes
Sumit Puri	Fujitsu	P	Yes
Andrew Vuong	Hitachi	P	Yes
	IBM		Did not vote
Michael Eschmann	Intel	P	Yes with comments
Tim Bradshaw	Iomega	P	Yes
Andre Hedrick	Linux ATA Development	P	Yes
Tim Thompson	LSI Logic	P	Yes
Pete McLean	Maxtor	P	Yes with comments
Nita Pan	Microsoft	A	Yes with comments
	Morgan Link		Did not vote
Tony Goodfellow	Pacific Digital	P	Yes
	Phoenix Technologies		Did not vote
	Qlogic		Did not vote
Bob Chang	Sandisk	P	Yes
Marc Noblitt	Seagate	P	Yes
Aaron Wilson	ST Microelectronics	P	Yes
Tasuku Kasebayashi	Toshiba	P	Yes
Darrin Bulik	Western Digital	P	Yes

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NCITS Secretariat: Information Technology Industries Council (ITI)

1250 Eye Street, N.W., Suite 200, Washington, DC 20005-3922; Fax: (202) 638-4922 Tel: (202) 737-8888

Three yes votes included comments. These comments are enclosed.

Regards,

P.T. McLean
T13 Chairman

Enclosure 1 – Comments

Enclosure 1

Comments accompanying Intel Yes vote on letter ballot to forward EDD-2.

1. **Section 3.2.21:** Section should be called “Protected Mode”.
2. **Section 6.8.1, Table 4:** Change table to remove intermediate borders for PCI-X group in “Host Bus Type” column.
3. **Section 6.8.2, Table 5:** Make same intermediate border change as in suggestion #2.
4. **Section 6.8.3, Table 6:** Would really like to see text that relates LBA bits in offset 4 bit 6, offset 10 bits 4, 9 and 10, showing how a consumer of INT13 would interpret the results.

Comments accompanying Maxtor Yes vote on letter ballot to forward EDD-2.

Comment 1 – Contents

Contents entries should not be underlined.

Comment 2 – Forward

“Subcommittee T13 on ATA Interfaces, that reviewed this standard, had the following members:” should say “Technical Committee T13 on ATA Interfaces, that reviewed this standard, had the following members:”

Comment 3 – Clause 2.1 Approved References

There should be a space between 340-2000 and AT Attachment.

Comment 4 - Clause 3.2.5 CF

The word Carry should not be bold.

Comment 5 – 3.2.6 CHS

In the first sentence, “logical heads (S),” should be “logical heads (H),”.

Comment 6 – 3.2.6 CHS

Remove period in front of the last sentence.

Comment 7 – 3.2.7 Conventional and enhanced

Need space in front of the last sentence.

Comment 8 – 3.2.21 Protect Mode

Real Mode is defined in the Protect Mode entry. Shouldn't Real Mode be its own definition entry?

Comment 9 – 5.3 INT 13h Interface Subsets

In the note, "INT 13" should be "INT 13h".

Comment 10 – 5.3 INT 13h Interface Subsets

The note needs a period at the end.

Comment 11 – 5.3.2 Device Locking and Ejecting Subset

In the last item in the table "Int 15h" should be "INT 15h".

Comment 12 – 6.5 Lock/Unlock Media

The parenthetic statement "(ie. AH = 00h and CF = 0b)" should be "(i.e., AH = 00h and CF = 0b)".

Comment 13 – 6.6 Eject Removable Media

Parenthetic statements "(ie., ----)" should be "(i.e., -----)" in four places.

Comment 14 - 6.6 Eject Removable Media

In the last sentence, "Int 15h" should be INT 15h".

Comment 15 – 6.8 Get Device Parameters – Table 3

Offset 2, bit 7, "Int 13h" should be "INT 13h".

Comment 16 – 6.8.1 Interface Path – Table 4

In PCI offset 52 and PCI-X offset 52, if these are DWords the value should be 00000000h.

Comment 17 – 6.8 3 Device Parameter Table Extension (DPTE) – Table 6

In offset 10-11, bits 12-15, the last word should be "zero".

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Microsoft approves the EDD-2 spec with four comments and a question.

Comments:

- 1) In Section 6.3 Extended write, 1st paragraph, 2nd sentence, it should be:

"CF = 1b"

2) In section 6.8.1 Interface Path, table 4:

a) The definition for Host bus Type: PCI, Offset 52, should be written as: "Reserved. The value in this field shall be 00000000"

b) The definition for Host bus Type: PCI-X, Offset 52, should be written as: "Reserved. The value in this field shall be 00000000"

3) In section 6.8 "Get Device Parameters" - offset 36, host bus type, probably should include 3GIO (or whatever it eventually gets called).

4) Likewise, section 6.8, offset 40, probably should add InfiniBand. For InfiniBand, the interface type should be IB SRP and contain 128 bit target ID.

Question:

In section 6.8.2 Device Path, Table 5 - Device Path Definition:

The definition for Interface Type SATA, offset is "00h = SATA Device 0, 01h = SATA Device 1". Does that imply that master and slave channel in Serial ATA?

According to Intel, Serial ATA does NOT have the concept of master and slave. It only supports one channel.