

**Proposed
Draft**

**T13
xxxxDT**

**Revision 000
25 March 2004**

Technical Report: Time-Limited Commands (TLC)

This is an internal technical report of T13, a Technical Committee of Accredited Standards Committee INCITS. As such, this is not a completed technical report and has not been approved. The contents may be modified by the T13 Technical Committee. This technical report is made available for review and comment only.

Permission is granted to members of INCITS, its technical committees, and their associated task groups to reproduce this document for the purposes of INCITS standardization activities without further permission, provided this notice is included. All other rights are reserved. Any commercial or for-profit replication or republication is prohibited.

T13 Technical Editor:

Jim Hatfield
Seagate Technology LLC
389 Disc Drive
Longmont, CO 80503
USA

Tel: 720-684-2120
Fax: 720-684-2711

Reference number
ANSI INCITS.*** - xxxx
Printed March, 26, 2004 3:40PM

Other Points of Contact:

T13 Chair
Dan Colgrove
Hitachi Global Storage Technologies
2903 Carmelo Dr
Henderson, NV 89502
Tel: 702-614-6119
Fax: 702-614-7955

T13 Vicechair
Jim Hatfield
Seagate Technology
389 Disc Drive
Longmont CO 80503
Tel: 720-684-2120
Fax: 720-684-2711

INCITS Secretariat
Administrator Standards Processing
1250 Eye Street, NW Suite 200
Washington, DC 20005
Tel: 202-737-8888
Fax: 202-638-4922
Email: INCITS@ITIC.ORG

T13 Reflector

See the T13 Web Site at <http://www.t13.org> for reflector information.

T13 Web Site

<http://www.t13.org>

T13 Anonymous FTP Site

<ftp.t13.org>

T13 mailings

Global Engineering
15 Inverness Way East
Englewood, CO 80112-5704
Tel: 303-792-2181 or 800-854-7179
Fax: 303-792-2192

DOCUMENT STATUS

Revision 0 – March 25, 2004

Document created from proposal E03117R2.
Added editorial changes requested

American National Standard
for Information Technology —

Technical Report:
Time-Limited Commands
(TLC)

Secretariat
Information Technology Industry Council

Approved mm dd yy

American National Standards Institute, Inc.

Abstract

The purpose of the Time-Limited Commands (TLC) feature set is to define a mode of operation that balances streaming performance with reliability.

NCITS's Technical Report Series

This Technical Report is one of a series produced by the American National Standards Committee, NCITS, Information Technology. The secretariat for NCITS is held by Information Technology Industry Council (ITI), 1250 Eye Street, NW Suite 200, Washington DC 20005.

As a by-product of the standards development process and the resources of knowledge devoted to it, NCITS from time to time produces Technical Reports. Such Technical Reports are not standards, nor are they intended to be used as such.

NCITS Technical Reports are produced in some cases to disseminate the technical and logical concepts reflected in standards already published or under development. In other cases, they derive from studies in areas where it is found premature to develop a standard due to still changing technology, or inappropriate to develop a rigorous standard due to the existence of a number of viable options, the choice of which depends on the user's particular requirements. These Technical Reports, thus, provide guidelines, the use of which may result in greater consistency and coherence of information processing systems.

When the draft Technical Report is completed, the Technical Committee approval process is the same as for a draft standard. Processing by NCITS is also similar to that for a draft standard.

CAUTION: The developers of this Technical Report have requested that the holder's of patents that may be required for the implementation of this Technical Report, disclose such patents to the publisher. However, neither the developers nor the publisher have undertaken a patent search in order to identify which, if any, patents may apply to this Technical Report. As of the date of this Technical Report and the following calls for the identification of patents that may be required for the implementation of the Technical Report, no such claims have been made. No further patent search is conducted by the developer or the publisher in respect to any Technical Report it Processes. No representation is made or implied that licenses are not required to avoid infringement in the use of this Technical Report.

Published by
American National Standards Institute
11 West 42nd Street, New York, New York 10036

Copyright nnnn by American National Standards Institute
All rights reserved.

Contents	Page
1 Scope	1
1.1 Assumptions	1
2 Normative references	1
2.1.1 Approved references	1
2.1.2 References under development	1
2.1.3 Other references	1
3 Definitions, abbreviations, and conventions	2
3.1 Definitions and abbreviations	2
3.1.1 AbortMode	2
3.1.2 CCTL	2
3.1.3 Command Timer	2
3.1.4 DWE	2
3.1.5 NormalMode	2
3.1.6 Qualified TLC command	2
3.1.7 Re-arm the timer	2
3.1.8 RC	2
3.1.9 ReadContinuous Mode	2
3.1.10 SE	2
3.1.11 Timer armed	2
3.1.12 Timer expired	2
3.1.13 Timer running	3
3.1.14 TLC Mode	3
3.1.15 WC	3
3.1.16 WriteContinuous Mode	3
3.2 Conventions	3
3.2.1 Conventions are defined elsewhere	3
4 Description of the Feature Set	4
4.1 TLC feature set	4
4.2 Command Completion Timer	4
4.3 Commands Affected	4
4.4 Operational Summary	4
4.4.1 Host Behaviour	4
4.4.2 Device Behaviour	5
4.5 State Diagrams	6
4.5.1 Time-Limited Command Overview	6
4.5.2 Time-Limited Flush Cache Command	8
4.5.3 TLC Error Handling	10
4.6 Changes to Host Adapter Registers	13
4.6.1 Error register	13
4.7 Changes to Commands	13
4.7.1 Commands Affected	13
4.7.2 FLUSH CACHE	14
4.7.3 FLUSH CACHE EXT	15
4.7.4 IDENTIFY DEVICE	17
4.7.5 READ DMA	18
4.7.6 READ DMA EXT	19
4.7.7 READ LOG EXT	21
4.7.8 SET FEATURES	22
4.7.9 WRITE DMA	23
4.7.10 WRITE DMA EXT	25

Figures	Page
Figure 1 - TLC Overview State Diagram	6
Figure 2 - TLC Flush Cache State Diagram	8
Figure 3 - TLC Error Handling State Diagram	10

Foreword

This technical report describes the Time-Limited Commands (TLC) feature.

This technical report was developed by T13 during 2004. The approval process started in 2xxx. This document is not an American National Standard and the material contained herein is not normative in nature. Comments on the content of this document should be sent to the NCITS Secretariat, Information Technology Industry Council, 1250 Eye Street, NW (Suite 200), Washington, DC 20005.

(This technical report was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, NCITS. Committee approval of the technical report does not necessarily imply that all committee members voted for approval. At the time it approved this technical report, the NCITS Committee had the following members:)

Dan Colgrove, Chairman
Jim Hatfield, Vice-Chairman
Mark Overby, Secretary

Organization Represented Name of Representative

Technical Committee T13 on ATA Interfaces, that reviewed this standard, had the following members:

Technical Committee T13 on ATA Interfaces, that developed this standard, had the following additional participants:

Introduction

This technical report encompasses the following:

Clause 1 describes the scope.

Clause 2 provides normative references for the entire technical report.

Clause 3 provides definitions, abbreviations, and conventions used within the entire standard.

Clause 4 describes the Time-Limited Commands feature

National Committee for Information Technology Standards (NCITS) Technical Report —

Time-Limited Commands (TLC)

1 Scope

1.1 Assumptions

This feature set is optional for devices not implementing the PACKET Command feature set and prohibited for devices implementing the PACKET Command feature set.

2 Normative references

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax), or via the World Wide Web at <http://www.ansi.org>.

Additional availability contact information is provided below as needed.

AT Attachment with Packet Interface Extension (ATA/ATAPI-7), [ANSI INCITS.xxx-2004]

2.1.1 Approved references

None.

2.1.2 References under development

None.

2.1.3 Other references

None.

3 Definitions, abbreviations, and conventions

3.1 Definitions and abbreviations

For the purposes of this technical report, the following definitions apply:

3.1.1 AbortMode

In this mode, if a stream error occurs, the device shall immediately abort the current command, even aborting any data transfer currently in process.

3.1.2 CCTL

Command Completion Time Limit is the time limit (set via SET FEATURES) that the TLC feature set uses.

3.1.3 Command Timer

The Command Timer is a timer that begins running on receipt of the first qualified READ or WRITE command after the timer is 'armed' (see below), and continues until completion of a FLUSH CACHE or FLUSH CACHE EXT command. While the timer is running, the host may send any number (or type) of commands to the device. These commands may be qualified TLC commands or any other commands.

3.1.4 DWE

Deferred Write Error is flagged if the Command Timer expires during a qualified WRITE or FLUSH command.

3.1.5 NormalMode

Normal mode operations occur when the TLC Command Timer has a zero value (e.g. TLC mode is disabled).

3.1.6 Qualified TLC command

Only these commands have defined behaviour differences in TLC mode:
READ DMA, READ DMA EXT, WRITE DMA, WRITE DMA EXT, FLUSH CACHE, FLUSH CACHE EXT.

3.1.7 Re-arm the timer

Pre-load the timer with the selected CCTL value.

3.1.8 RC

See 'ReadContinuous Mode'

3.1.9 ReadContinuous Mode

In this mode, if a stream error occurs, the device shall continue to send data to the host, and the host shall understand that the data may be invalid. The purpose is to maintain a steady state of stream activity, regardless of the quality of the data.

3.1.10 SE

Stream Error is flagged when the Command Timer expires during the execution of a qualified TLC command.

3.1.11 Timer armed

The Command Timer is 'armed' (but not 'running') after:

- a) a SET FEATURES command is received to define it as a non-zero value (or)
- b) a FLUSH CACHE or FLUSH CACHE EXT command completes

3.1.12 Timer expired

The Command Timer is 'expired' after the CCTL period of time elapses from the time that the timer enters the 'running' state.

3.1.13 Timer running

The Command Timer begins 'running' on receipt of the first qualified READ or WRITE command after the timer is 'armed'.

3.1.14 TLC Mode

Time-Limited Command mode is active when a non-zero CCTL value has been set vis SET FEATURES.

3.1.15 WC

See 'WriteContinuous Mode'

3.1.16 WriteContinuous Mode

In this mode, if a stream error occurs, the device shall continue to accept data from the host, and the device shall understand that the data may be invalid. The purpose is to maintain a steady state of stream activity, regardless of the quality of the data.

3.2 Conventions

3.2.1 Conventions are defined elsewhere

See ATA/ATAPI-7 for conventions to be used.

4 Description of the Feature Set

4.1 TLC feature set

The basic idea is for the host to define (to the device) a maximum time limit during which a group of commands is expected to complete. The device shall attempt to guarantee completion (of the group of commands) within the time limit.

4.2 Command Completion Timer

The timer (in the device) has these mutually exclusive states: disabled, armed, running. The timer may be expired but still running.

The timer does NOT apply to each individual command, but to the combined time required to execute a 'group' of commands. If the device does not complete a qualified command (e.g. clear BSY to zero) before the timer expires, the device shall either abort the command or continue (possibly transferring incorrect data).

4.3 Commands Affected

This mode applies only to these qualified commands which are subject to the Command Completion Time Limit (CCTL):

- FLUSH CACHE
- FLUSH CACHE EXT
- READ DMA
- READ DMA EXT
- WRITE DMA
- WRITE DMA EXT

In addition, these commands contain support for TLC feature set:

- IDENTIFY DEVICE
- READ LOG EXT
- SET FEATURES

4.4 Operational Summary

4.4.1 Host Behaviour

When this feature is supported by the device:

The Host:

1. may terminate this mode by executing a SET FEATURES command to set a zero value for a CCTL;
2. may enter this mode by executing a SET FEATURES command to set a *non-zero* value for a CCTL;
3. may execute a SET FEATURES command to specify the action to be taken by the device if a command does not complete within the define time window (e.g. abort or continue with bad data: 'ReadContinuous (RC) / WriteContinuous (WC)' option)
4. shall 'arm' the timer for the first group of commands by executing a FLUSH CACHE [EXT] command, knowing that the timer does not start until the host sends the first qualified READ or WRITE command to the device;
5. shall execute each group of commands with this protocol:
 - a. execute a qualified READ or WRITE command on the device. The first such command after a FLUSH CACHE [EXT] command starts the Command Completion Timer.

- b. execute any group of commands to the device. The number and type of commands in this group depends on the expected average completion time (for the specific commands on this specific device) and on the selected CCTL value;
- c. expect that the group of READ and/or WRITE qualified commands shall complete before the time limit expires. Commands other than those listed above shall not be affected by the CCTL.
- d. complete the execution of a FLUSH CACHE [EXT] command BEFORE the expiration of the time limit. This shall stop and re-arm the time for the next group of commands. If the timer expires DURING a Flush Cache command, the buffered data is not guaranteed to still be in the buffer. It should be considered as 'lost' or 'destroyed'. The host should re-issue all writes sent since the last FLUSH CACHE [EXT] command.

4.4.2 Device Behaviour

When this feature is supported by the device:

- 1. on completion of a FLUSH CACHE command shall stop the Command Completion Timer, re-arm it, but not allow it to run;
- 2. shall start the Command Completion Timer on receipt of the first qualified READ or WRITE command after a FLUSH CACHE [EXT] command
- 3. shall not allow the Command Completion Timer to affect the outcome of commands other than those listed above;
- 4. all qualified commands must complete before the CCTL expires. If the command cannot complete because of retries (or any other reason), it shall be terminated (either aborted or finished with incorrect data). The data returned may include the bad sector.
- 5. On receipt of a Power-on Reset or Hard Reset, the Stream Error logs (21h and 22h) shall be cleared of all recorded events.
- 6. On receipt of a Soft Reset, the Stream Error logs are unaffected.

When this feature is not supported or not enabled (e.g. Normal mode):

- 1. The WorstCase timer and the 'ReadContinuous (RC) / WriteContinuous (WC)' option are ignored (or not even implemented).
- 2. All configured retries shall be executed before an error is returned to the host.
- 3. If a Read command cannot complete because of retries, the data returned may include the bad sector.

4.5 State Diagrams

4.5.1 Time-Limited Command Overview

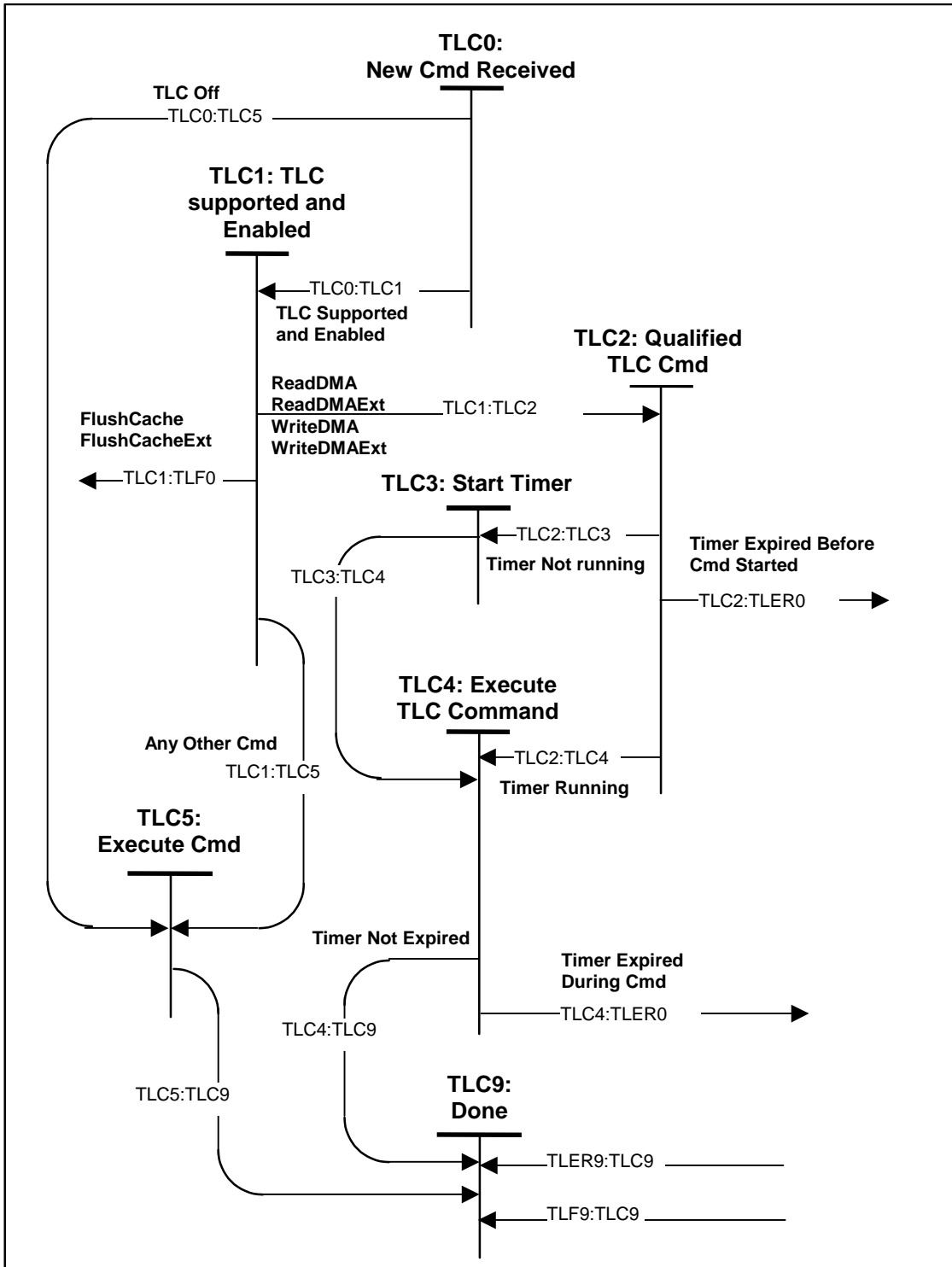


Figure 1 - TLC Overview State Diagram

TLC0: New Cmd Received: This state is entered when the device receives a new command from the host.

Transition TLC0:TLC1: This transition shall be taken if TLC mode is both supported and enabled.

Transition TLC0:TLC5: TLC mode is either not supported or not enabled.

TLC1: TLC supported and enabled: This state is entered when TLC mode is both supported and enabled.

Transition TLC1:TLF0: The command is either FLUSH CACHE or FLUSH CACHE EXT

Transition TLC1:TLC2: The command is either READ DMA, READ DMA EXT, WRITE DMA, or WRITE DMA EXT.

Transition TLC1:TLC5: The command is not a qualified TLC command.

TLC2: Qualified TLC Cmd: The command is known to be a Read or Write command that is affected by TLC feature set.

Transition TLC2:TLC3: If the timer is not running, the timer shall be started.

Transition TLC2:TLC4: If the timer is already running, the command shall be executed.

Transition TLC2:TLER0: If the timer has expired, Time-Limited error handling shall take place.

TLC3: Start Timer: Prior to entering this state, the timer has been loaded with the appropriate value. The timer is now started.

Transition TLC3:TLC4: The command shall be executed.

TLC4: Execute TLC Cmd: The command shall be executed. The timer shall be checked at times during execution.

Transition TLC4:TLC9: The timer did not expire during the execution of the command.

Transition TLC4:TLER0: The timer expired during the execution of the command. Time-Limited error handling shall take place.

TLC5: Execute Other Cmd: The command shall be executed without checking the timer either before, during or after execution. This state of the timer is not affected.

Transition TLC5:TLC9: Proceed to Normal end-of-command.

TLC9: Done: Normal end-of-command processing happens here

4.5.2 Time-Limited Flush Cache Command

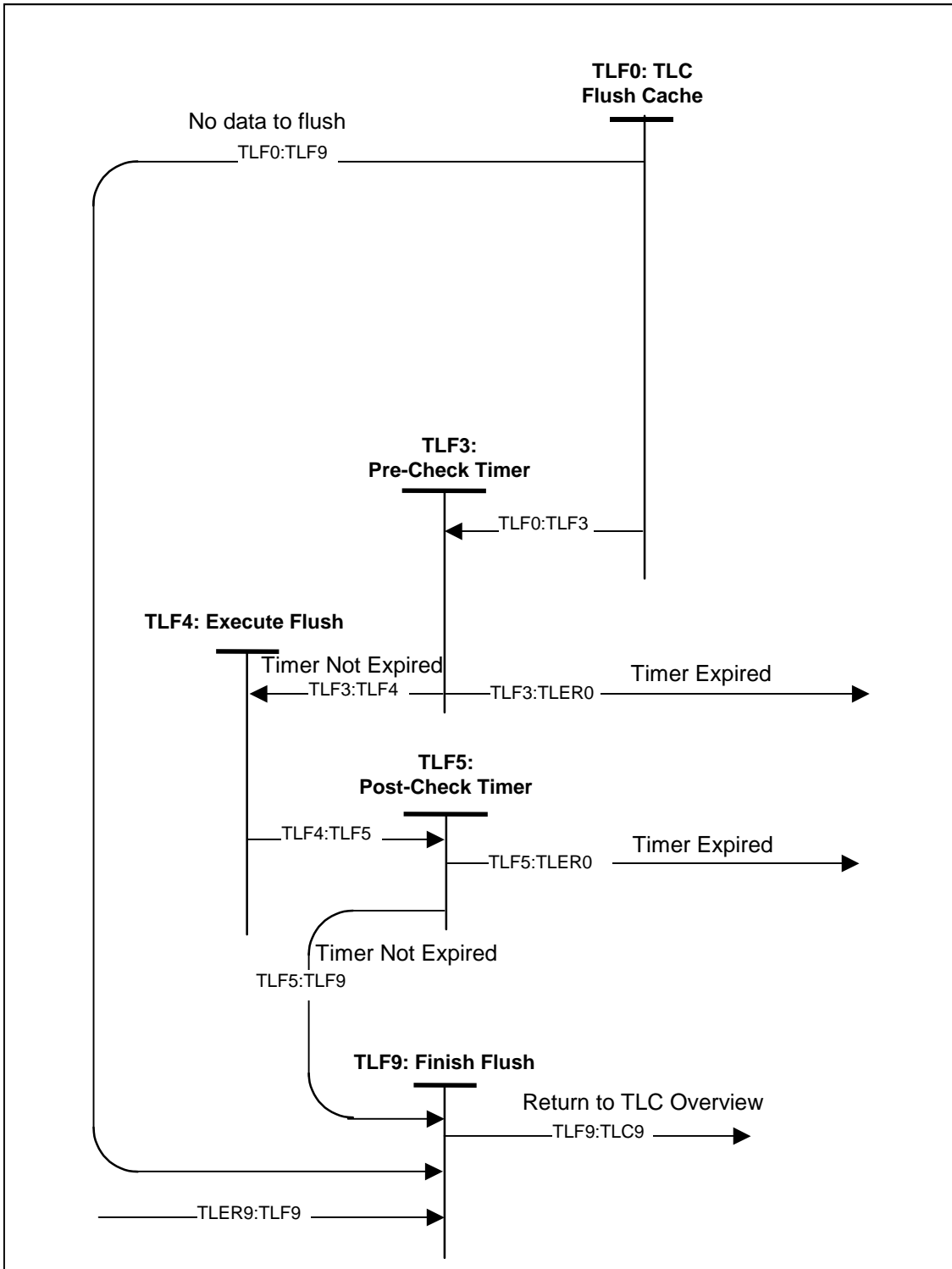


Figure 2 - TLC Flush Cache State Diagram

TLF0: TLC Flush Cache: While in TLC Mode, a FLUSH CACHE or FLUSH CACHE EXT command was received by the device.

Transition TLF0: TLF3 : If there are data to flush, continue.

Transition TLF0:TLF9: If there are no data to flush, proceed to the Flush Done state.

TLF3: Pre-Check Timer: Before executing the FLUSH command, see if the timer has expired.

Transition TLF3:TLF4: If the timer has not already expired, the FLUSH command shall be executed.

Transition TLF3:TLER0: The timer has already expired. Time-Limited error handling shall be performed.

TLF4: Execute Flush: The FLUSH command shall be executed. The timer shall be checked at times during execution.

Transition TLF4:TLF5: When the FLUSH operation is done, the timer shall be checked again.

TLF5: Post-Check Timer: See if the timer expired during the FLUSH operation.

Transition TLF5:TLF9: The timer has still not expired. Proceed to normal completion.

Transition TLF5:TLER0: The timer expired during the FLUSH. Time-Limited error handling shall be performed.

TLF9: Finish Flush: Stop the timer. Re-arm the TLC timer.

Transition TLF6:TLC9: Proceed to normal Time-Limited Command completion.

4.5.3 TLC Error Handling

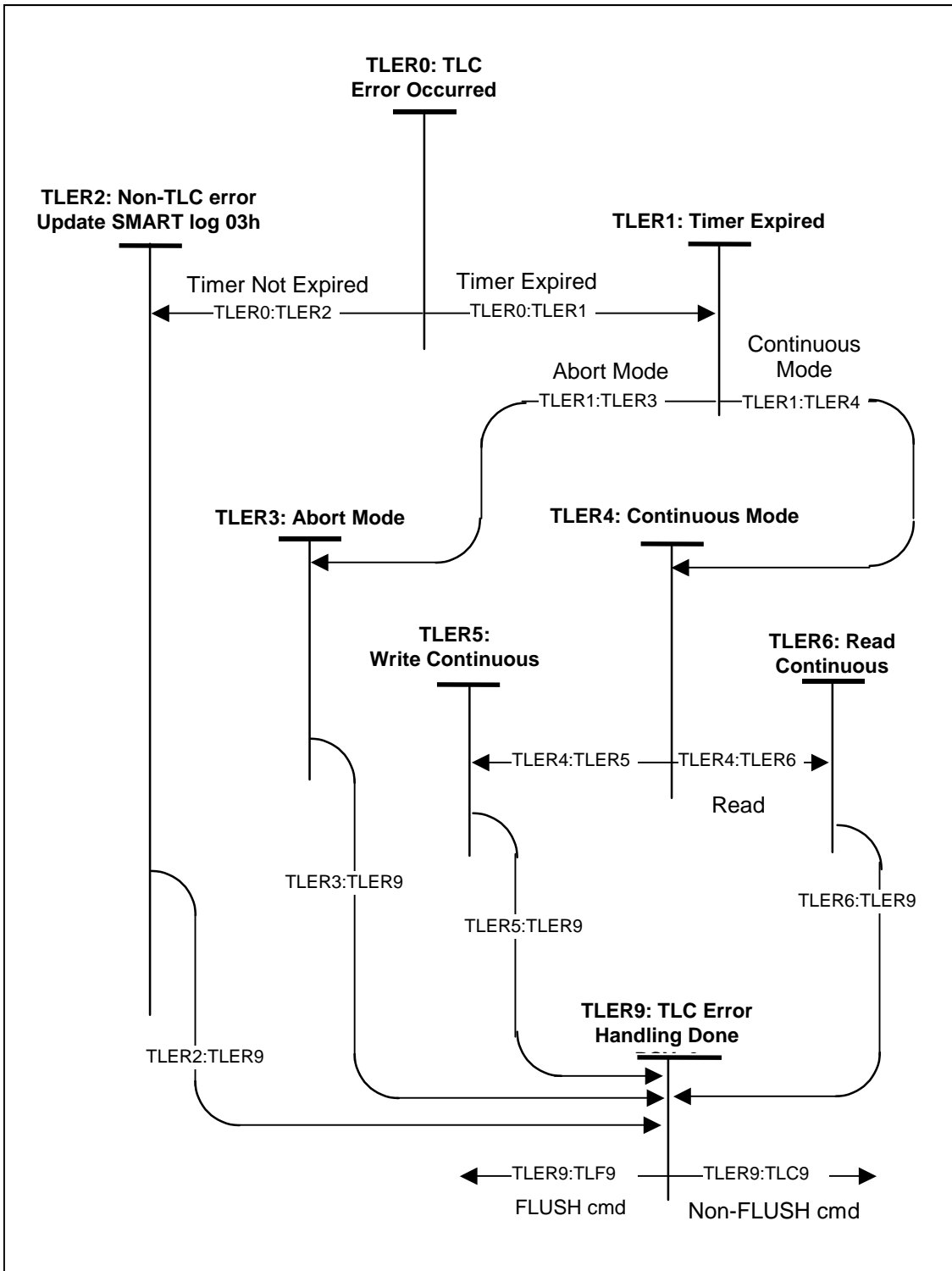


Figure 3 - TLC Error Handling State Diagram

TLER0: TLC Error Occurred: This state is entered when the timer has expired and the command has decided to report a timeout error.

Note: Previously buffered data is not guaranteed to still be in the buffer. The host should re-issue all writes attempted since the last successful FLUSH CACHE [EXT] command.

Transition TLER0:TLER1: The error is that the timer expired. Report the error as below.

Transition TLER0:TLER2: The error is not related to the timer expiring. Report the non-AV error in SMART log 03h.

TLER1: Timer Expired: The timer expired. Stop the timer.

Transition TLER1:TLER3: A SET FEATURES command put the device into 'Time-Limited Abort' mode.

Transition TLER1:TLER4: A SET FEATURES command put the device into 'TLC Continuous' mode.

TLER2: Non-TLC Error: Set the ERROR register to a non-zero value. Set ERR to one, clear BSY to zero. Report the non-AV error in SMART log 03h.

Transition TLER2:TLER9: Proceed to end-of-command processing.

TLER3: Abort Mode: Terminate any active data transfer immediately. Set STATUS register bit ERR to one, clear SE to zero. If this is a WRITE command, set DWE to one. Set the ERROR register to a non-zero value. Previously buffered data is not guaranteed to still be in the buffer. Since all data may not have been transferred, a host bus master underrun may occur. The host must treat this as an allowable expectable event.

Transition TLER3:TLER9: Proceed to end-of-command processing.

TLER4: Continuous Mode: Set STATUS register bit SE to one, clear ERR to zero. Set the LBA registers to the LBA of the first LBA in error. Set the SECTOR COUNT register to the number of sectors in error. Clear the ERROR register to zero.

Transition TLER4:TLER5: Take this transition if the current command is WRITE DMA, WRITE DMA EXT, FLUSH CACHE or FLUSH CACHE EXT.

Transition TLER4:TLER6: Take this transition if the current command is READ DMA or READ DMA EXT.

TLER5: Write Continuous: A WRITE DMA [EXT] or FLUSH CACHE [EXT] command was active when the Command Timer expired. Finish accepting the remainder of the outstanding data from the host. Set STATUS register bit DWE to one. Clear BSY to zero. Log the error in SMART log 21h (Write Stream Log) when time permits. The data just transferred and previously buffered data is not guaranteed to still be in the buffer.

Transition TLER5:TLER9: Proceed to end-of-command processing.

TLER6: Read Continuous: A READ DMA [EXT] command was active when the Command Timer expired. Continue to transmit the remainder of the (potentially incorrect) data to the host, up to the expected transfer count. Clear BSY to zero. Log the error in SMART log 22h (Read Stream Log) when time permits. The host must expect that the data will miscompare, and allow for that event.

Transition TLER6:TLER9: Proceed to end-of-command processing.

TLER9: TLC Error Handling Done:

Transition TLER9:TLC9: Proceed to normal Time-Limited Command completion.

4.6 Changes to Host Adapter Registers

4.6.1 Error register

4.6.1.1 Access restrictions

The contents of this register shall be valid when BSY and DRQ are cleared to zero and either ERR or SE are set to one. The contents of this register shall be valid upon completion of power-on, or after a hardware or software reset, or after command completion of an EXECUTE DEVICE DIAGNOSTICS or DEVICE RESET command. The contents of this register are not valid while a device is in the Sleep mode.

4.7 Changes to Commands

4.7.1 Commands Affected

Changes shall be made to the following commands :

- FLUSH CACHE
- FLUSH CACHE EXT
- IDENTIFY DEVICE
- READ DMA
- READ DMA EXT
- READ LOG EXT
- SET FEATURES
- WRITE DMA
- WRITE DMA EXT

4.7.2 FLUSH CACHE

4.7.2.1 Change to Error outputs

An unrecoverable error encountered during execution of writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE commands continue the process of flushing the cache starting with the first sector after the sector in error.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF / SE	na	DRQ	na / DWE	na	ERR

Error register –

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, LBA High, Device –

shall be written with the address of the first unrecoverable error. If the device supports the 48-bit Address feature set and the error occurred in an address greater than FFFFFFFh, the value set in the LBA Low, LBA Mid, and LBA High registers shall be FFh and the value set in bits (3:0) of the Device register shall be Fh.

Device register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero

DWE (Deferred Write Error) shall be set if the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command. If DWE is set to one and SE is cleared to zero, the values in the Sector Count, LBA Low, LBA Mid, and LBA High registers are undefined.

4.7.3 FLUSH CACHE EXT

4.7.3.1 Change to Error outputs

An unrecoverable error encountered while writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE EXT commands continue the process of flushing the cache starting with the first sector after the sector in error.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	na
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF / SE	na	DRQ	na / DWE	na	ERR
NOTE – HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register -

ABRT shall be set to one if the device is not able to complete the action requested by the command.

LBA Low -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

LBA Mid -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

LBA High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB is set to one.

Device register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

DWE (Deferred Write Error) shall be set if the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE EXT command.. If DWE is set to one and SE is cleared to zero, the values in the Sector Count, LBA Low, LBA Mid, and LBA High registers are undefined.

4.7.4 IDENTIFY DEVICE

4.7.4.1 Change to Table 27

116	O	V	Number of ms (in 10 msec increments) for the Command Completion Timer in the TLC feature set
-----	---	---	--

4.7.4.2 Change to Words (84:82): Features/command sets supported

If bit 11 of word 84 is set to one, The device supports the TLC feature set.

If bit 12 of word 84 is set to one, the device supports the Read Continuous and Write Continuous mode within the TLC feature set.

4.7.4.3 Change to Word 116: Command Completion Time Limit (CCTL) for TLC feature set

If the TLC feature set is supported and enabled, this word equals the number of milliseconds (in 10 msec increments) that the CCTL has been initialized to, e.g., a value of 70 indicates a 700 ms CCTL.

4.7.5 READ DMA

4.7.5.1 Change to Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	Length of error (7:0)							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF / SE	na	DRQ	na	na	ERR

Error register –

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device.

This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count – shall indicate the number of contiguous sectors containing potentially bad data beginning with the LBA of the first sector with an uncorrectable error if the TLC feature set is supported and enabled.

LBA Low, LBA Mid, LBA High, Device –

shall be written with the address of first unrecoverable error.

Device register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

4.7.6 READ DMA EXT

4.7.6.1 Change to Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Length of error (7:0)							
	HOB = 1	Length of error (15:8)							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF / SE	na	DRQ	na	na	ERR
NOTE – HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register –

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count –

bits (7:0) contain the number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an error when read with Device Control register HOB bit cleared to zero.

bits (15:8) contain the number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an error when read with Device Control register HOB bit set to one.

LBA Low –

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid –

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High –

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

4.7.7 READ LOG EXT

4.7.7.1 TLC feature set errors

Write stream errors shall be placed in log 21h. Read stream errors shall be placed in log 22h.

Data for this log is temporarily saved whenever a timeout occurs. As workload permits, this data shall be written to the READ LOG EXT Log 21h or 22h. This logging of errors is not to affect performance. Performance during TLC operation is more critical than Error Logging. If this means that errors fail to log, then some errors shall not be logged. This being stated, if the Error Log can be updated for future reporting without affecting performance, it should be done.

The purpose of this log is to give the host a list of errors on the drive that can be reallocated or not accessed in the future. The host shall be able to reallocate these sectors by writing to them in normal (not TLC feature set) mode. The host may also choose simply not to access these LBA's via its own algorithms.

On receipt of a Power-on or Hard Reset, Write Stream and Read Stream logs shall be cleared of all recorded events.

'Cleared' means: the log version numbers shall be correct, and all counts and indices shall be cleared to zeros.

After the host reads the Write Stream log, the device shall clear the Write Stream log. After the host reads the Read Stream log, the device shall clear the Read Stream log.

4.7.8 SET FEATURES

4.7.8.1 Changes to Table 41 – “SET FEATURES register definitions”

Value (see note)	
20h	Reserved for technical report Set TLC CCTL
21h	Reserved for technical report Set TLC Error Handling

4.7.8.2 Set TLC CCTL

This is only valid if the TLC feature set is supported.

Example:

The Sector Count set to 70 indicates a 700 millisec CCTL.

Notes –

1. The host initializes the Sector Count register with the desired value.
2. The Command Completion Timer shall be cleared to zero on any reset.
3. A value of zero in the Sector Count register shall disable the TLC feature set, and shall clear bit 11 to zero in word 87 of the IDENTIFY DEVICE response.
4. A non-zero value shall set bit 11 to one in word 87 of the IDENTIFY DEVICE response. In addition, this will arm (but not start) the Command Completion Timer.
5. A manufacturer may modify any timer set below it's minimum retry time to that drives minimum retry time. (e.g. if the user attempts to set this to 10 ms and the manufacturer has a minimum retry time of 200 ms, the drive's CCTL shall be set to 200 ms)
6. The effective CCTL value shall be displayed in Word 116 of the IDENTIFY DEVICE response.
7. This timer represents the maximum command completion time from the host perspective. The drive shall clear BSY to zero before this time limit expires. Internally, the actual time that shall trigger a timeout shall be shorter than this value to ensure that this value is not exceeded.

Register	7	6	5	4	3	2	1	0
Features	20h							
Sector Count	10 millisec increments of the CCTL							

4.7.8.3 Set TLC error handling

This is only valid if the TLC feature set is supported, and the TLC “ReadContinuous/WriteContinuous mode” is supported

This enables or disables “ReadContinuous (RC) / WriteContinuous (WC) mode” in the TLC feature set.

A value of zero in the Sector Count register shall clear bit 12 to zero of word 87 of the IDENTIFY DEVICE response and shall cause aborts if the TLC Timer expires on a R/W command.

A value of one in the Sector Count register shall set bit 12 to one in word 87 of the IDENTIFY DEVICE response and shall cause potentially incorrect data to be transferred if the Timer expires .

Register	7	6	5	4	3	2	1	0
Features	21h							
Sector Count	0 = Abort; 1 = ReadContinuous / WriteContinuous							

4.7.9 WRITE DMA

4.7.9.1 Change to Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF / SE	na	DRQ	DWE	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count – shall indicate the number of contiguous sectors containing potentially bad data beginning with the LBA of the first sector with an uncorrectable error if the TLC feature set is supported and enabled.

LBA Low, LBA Mid, LBA High, Device -

shall be written with address of first unrecoverable error.

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

DWE (Deferred Write Error) shall be set if the TLC feature set is supported and enabled.. If DWE is set to one and SE is cleared to zero, the values in the Sector Count, LBA Low, LBA Mid, and LBA High registers are undefined.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

4.7.10 WRITE DMA EXT

4.7.10.1 Change to Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		ICRC	WP	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Length of error (7:0)							
	HOB = 1	Length of error (15:8)							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	DWE	na	ERR
NOTE – HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer.

The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count –

bits (7:0) contain the number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an error when read with Device Control register HOB bit cleared to zero.

bits (15:8) contain the number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an error when read with Device Control register HOB bit set to one.

LBA Low -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SE (Stream Error) shall be set to one if an Error register bit is set to one, and the TLC feature set is supported and enabled, and the Command Completion timer expired prior to or during the FLUSH CACHE command, and the TLC Continuous mode is enabled. In this case the LBA returned in LBA Low, LBA Mid, and LBA High shall be the the address of the first sector potentially in error and the Sector Count register shall contain the number of consecutive sectors that may contain errors.

DWE (Deferred Write Error) shall be set if the TLC feature set is supported and enabled.. If DWE is set to one and SE is cleared to zero, the values in the Sector Count, LBA Low, LBA Mid, and LBA High registers are undefined.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero