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Information technology - AT Attachment 8 - ATA/ATAPI Serial Transport (ATA8-AST)

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ABSTRACT

This standard specifies the AT Attachment command set between host systems and storage devices. It provides a common command set for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices. It includes the PACKET feature set implemented by devices commonly known as ATAPI devices. This standard maintains a high degree of compatibility with the AT Attachment Interface with Packet Interface - 7 (ATA/ATAPI-7) volume 1, INCITS 397-2004, and while providing additional functions, is not intended to require changes to devices or software that comply with previous T13 standards.

Draft

American National Standard

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The patent statement goes here.

If no patents have been disclosed place the statement in 5.5.2 shall be used.

If any patents have been disclosed place the statement in 5.5.3 shall be used.

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Document f10107 is the issues list for this draft. f10107 contains a list of the issues associated with the document, an issue number that remains assigned to the issue for the life of document development, a resolution to the issue, an owner for the issue, and a disposition for the issue. All major changes associated with this draft starting with Rev 1 are first documented in f10107 and given a number. This includes proposals which are targeted for inclusion into this draft.

Revision History		
Rev	**Date**	**Description**
1	August 16, 2007	1) Used ATA8-ACSr4b as a template to port ATA8-ASTr0 + Changes to this version. This version should be taken as the initial proposal...
2	October 21, 2009	2) New Editor starting cleanup. There are no proposals integrated in this version. This version supersedes the previous initial proposals as the new initial proposal.
3	February 25, 2010	3) Updated Issues document reference, added Acronym Section (3.2), replaced clause 4 with material accepted in T13 plenary meetings (2010-02)

New Capabilities added to ATA8-AST

Integrated Proposal List		
#	**Doc**	**Description**
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Foreword

(This foreword is not part of this standard.)

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, ITI, 1101 K Street NW, Suite 610, Washington, DC 20005.

This standard was processed and approved for submittal to ANSI by InterNational Committee for Information Technology Standards (INCITS). Committee approval of this standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, INCITS had the following members:

Karen Higginbottom, Chair

David Michael, Vice-chair

Monica Vago, Secretary

Technical Committee T13 on ATA Interfaces, that reviewed this standard, had the following members and additional participants:

Dan Colegrove, Chairman

Jim Hatfield, Vice-Chairman

Mark Overby, Secretary

Editor's Note 1: [Editors Note: Insert T13 Membership List Here]

Introduction

This standard encompasses the following:
Clause 1 describes the scope.
Clause 2 provides normative references for the entire standard.
Clause 3 provides definitions, abbreviations, and conventions used within the entire standard.
Clause 4 describes the mapping of ATA8-AAM and ATA8-ACS structures and resets into the Serial ATA transport

American National Standard
for Information Technology –

AT Attachment 8 - ATA/ATAPI Serial Transport (ATA8-AST)

1 Scope

The set of AT Attachment standards consists of this standard and the ATA implementation standards described in AT Attachment - 8 ATA/ATAPI Architecture Model (ATA8-AAM). ~~The scope of this standard is strictly limited the description of the mapping of ATA command structures, ATA command status (see ref. ATA8-ACS), ATA architecture model (see ref. ATA8-AAM), and ATA protocol model (see ref. ATA8-AAM) into the paradigm of the Serial ATA transport (see ref. Serial ATA Revision 2.6). The actual description of the Serial ATA transport, including, but not limited to, the description of:~~

~~a) the physical interconnection between Serial ATA host and Serial ATA storage device(s), including connectors and cables;~~
~~b) b) the electrical characteristics of the interconnecting signals;~~
~~c) c) the logical characteristics of the interconnecting signals; or~~
~~d) d) the protocols for transporting ATA commands, data, and status information using Serial ATA transport is not within the scope of this standard.~~

This document defines the ATA Serial ATA transport by:

a) referencing the Serial ATA documents published by the SATA-IO organization; and
b) documenting the transport dependent components found in ATA8 family of documents.

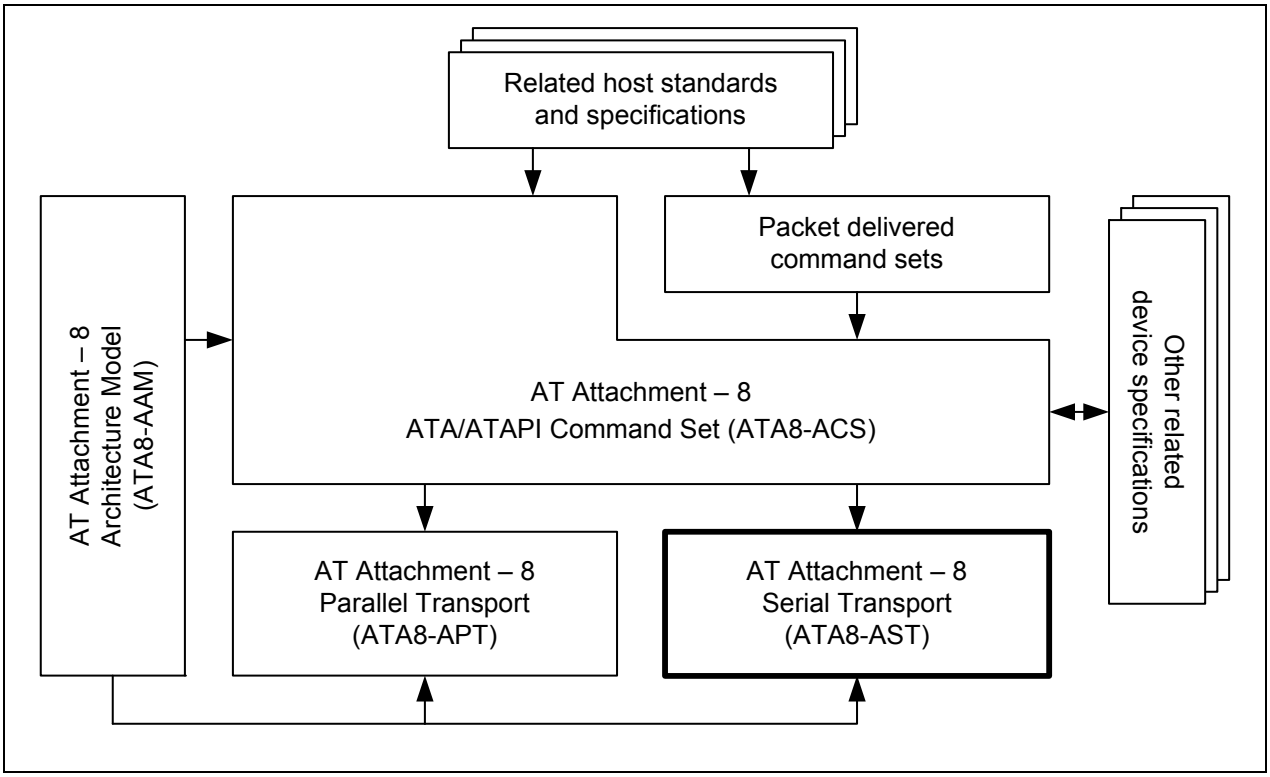
The following specifications are found in the SATA-2.6 and SATA-3.0 references:

a) the mapping of ACS-2 command blocks to SATA-3.0 FIS fields;
b) the physical interconnection between Serial ATA host and Serial ATA storage device(s), including connectors and cables;
c) the electrical characteristics of the interconnecting signals; and
d) the logical characteristics of the interconnecting signals.

This document specifies some of the relationship between this document and multiple versions of SATA. This document specifies:

a) the mapping of ACS-2 command blocks to SATA-2.6 FIS fields;
b) transport dependant command parameters (see ACS-2); and
c) transport dependant ATA transport dependent model components (see ATA8-AAM).

Figure 1 shows the relationship of this standard to the other standards and related projects in the ATA and SCSI families of standards and specifications. Note that the SATA-2.6 and SATA-3.0 documents exist outside of this specification framework.



Editor's Note 2: <Editor's Note: Update drawing for link between "related host..." and "other related...">

Figure 1 — ATA document relationships

2 Normative references

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents may be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax), or via the World Wide Web at http://www.ansi.org.

Additional availability contact information is provided below as needed.

2.1 Approved references

Table 1 lists approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them. To obtain copies of these documents, contact Global Engineering or INCITS. Additional information may be available at http://www.t10.org and http://www.t13.org

Table 1 — Approved ANSI References

Name	Reference
AT Attachment-8 – ATA Command Set (ATA8-ACS)	ANSI INCITS 452:2008
SCSI Primary Commands - 3 (SPC-3)	ANSI INCITS 408:2005 ISO/IEC 14776-453
AT Attachment-8 – ATA/ATAPI Architecture Model (ATA8-AAM)	ANSI INCITS 451:2008 ISO/IEC 14776-861

2.2 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

Table 2 — References Under Development

Name	Project Number
AT Attachment-8 - Parallel Transport (ATA8-APT)	INCITS 1698D ISO/IEC 14776-881
AT Attachment-8 – ATA/ATAPI Architecture Model (ATA8-AAM)	INCITS 1700D ISO/IEC 14776-861
AT Attachment-8 – ATA Command Set 2 (ACS-2)	INCITS 2015D
SCSI Primary Commands - 4 (SPC-4)	INCITS 1731D

For more information on the current status of the T10 documents, contact INCITS. To obtain copies of T10 or SFF documents, contact Global Engineering.

2.3 Other references

The following specifications are also referenced.

Serial ATA revision 2.6 (SATA-2.6)
Copies of the SATA 2.6 specification published by SATA-IO can be obtained at http://www.sata-io.org

Serial ATA revision 3.0 (SATA-3.0)
Copies of the SATA 3.0 specification published by SATA-IO can be obtained at http://www.sata-io.org

3 Definitions, abbreviations, and conventions

3.1 Definitions and abbreviations

Editor's Note 3: Review the use of each retained definition

3.1.1 28-bit command: A command which uses Features (7:0), Count (7:0), LBA (27:0), Device (15:8) and Command (7:0) to specify its arguments. (see 4.1)

3.1.2 48-bit command: A command which uses Features (15:0), Count (15:0), LBA (47:0), Device (15:8) and Command (7:0) to specify its arguments. (see 4.1)

~~**3.1.3 ASCII:** American Standard Code for Information Interchange.~~

~~**3.1.4 ASCII Character:** A byte containing a 7-bit ASCII pattern in bits 6:0 with bit 7 cleared to zero.~~

3.1.5 ATA device: A device implementing the ACS-2 General feature set.

3.1.6 ATA8-AST device: A device that complies with this standard.

3.1.7 ~~**ATAPI (AT Attachment Packet Interface) device:** ATAPI (AT Attachment Packet Interface) device: A device implementing the PACKET feature set.~~

3.1.8 ~~**BIOS (Basic Input/Output System):** An initial application client run by a computer when power is applied. The primary function of BIOS is initialize various components of the system, including storage devices.~~

3.1.9 byte: A sequence of eight contiguous bits considered as a unit. (See 3.3.8)

3.1.10 cache: A data storage area outside the area accessible by application clients that may contain a subset of the data stored in the non-volatile data storage area.

3.1.11 command aborted: Command completion with ERR set to one in the Status field and ABRT set to one in the Error field.

3.1.12 command acceptance: Positive acknowledgement of a command being received by a device. See the appropriate transport standard for a definition of positive acknowledgement.

3.1.13 command acceptance: Positive acknowledgement of a command being received by a device. See the appropriate transport standard for a definition of positive acknowledgement.

Editor's Note 4: **We need to define "positive acknowledgement" in the SATA domain**

3.1.14 Command Block: In a parallel implementation this is the set of interface registers used for delivering commands to the device or posting status from the device. In a serial implementation, the command block fields are FIS payload fields.

3.1.15 command completion: The completion by the device of the action requested by the command or the termination of the command with an error, the setting of the appropriate bits in the Error field, and the setting of the appropriate bits in the Status field.

3.1.16 command packet: A data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters.

3.1.17 command released: When a device supports the TCQ feature set, a command is considered released when a release occurs before command completion.

3.1.18 device: A storage-related peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.

3.1.19 ~~DMA (direct memory access) data transfer:~~ ~~A means of data transfer between device and host memory without host processor intervention.~~A method of data transfer between a host port and the device port which does not involve application client intervention.

3.1.20 DRQ data block: A unit of data words associated with available status when using either the PIO data-in command protocol or the PIO data-out command protocol.

3.1.21 Word: A sequence of four contiguous bytes considered as a unit. (See 3.3.8)

3.1.22 FIS: The Frame Information Structure for the serial interface. See SATA-2.6 and SATA-3.0.

3.1.23 hardware reset: ~~the routine performed by a device after a hardware reset event as defined in ATA8-AAM. The hardware reset routine performed by the device includes the actions performed by the device for a software reset, and the actions defined in ATA8-AAM, this standard, and the applicable transport standards.~~ The routine performed by a device after a hardware reset event as defined in ATA8-AAM or a COMRESET (see SATA 3.0). The hardware reset routine performed by the device includes the actions performed by the device for a software reset, and the actions defined in ATA8-AAM, this standard, and the appropriate SATA-IO specification (see SATA 3.0).

3.1.24 host: The computer system executing the application client (e.g., BIOS, operating system, or device driver) controlling the device and the adapter hardware for the ATA interface to the device.

3.1.25 ~~host adapter:~~ ~~The implementation of the host transport, link, and physical layers.~~

3.1.26 LBA (logical block address): The value used to reference a logical sector or a field used to carry a logical block address value.

3.1.27 ~~logical sector:~~ ~~A set of logical words accessed and referenced as a unit (see IDENTIFY DEVICE data words 118:117). These units are referenced by LBA (see).~~

3.1.28 ~~log:~~ ~~A collection of data accessed using log commands.~~

3.1.29 ~~log address:~~ ~~A numeric value that a log command uses to identify a specific log.~~

3.1.30 ~~log command:~~ ~~A SMART READ LOG command, SMART WRITE LOG command, or GPL feature set command.~~

3.1.31 ~~log page:~~ ~~A unit of measure for determining the size of a log. Each log page is a 512 byte block of data. A log consists of one or more pages.~~

3.1.32 LSB (least significant bit): In a binary code, the bit or bit position with the smallest numerical weighting in a group of bits that, when taken as a whole, represent a numerical value (e.g., in the number 0001b, the bit that is set to one).

3.1.33 ~~Master Password Capability: The Master Password Capability indicates whether or not the Master password may be used to unlock the device. This was formerly know as "Security Level".~~

3.1.34 ~~Media: The material on which data is stored.~~

3.1.35 ~~Media Access Command: Any command which causes the device to access non-volatile media.~~

3.1.36 MSB (most significant bit): In a binary code, the bit or bit position with the largest numerical weighting in a group of bits that, when taken as a whole, represent a numerical value (e.g., in the number 1000b, the bit that is set to one).

3.1.37 ~~native max address: The highest LBA that a device accepts in the factory default condition, that is, the highest LBA that is accepted by the SET MAX ADDRESS or, if the native max is greater than 28 bits then SET MAX ADDRESS EXT.~~

3.1.38 ~~Non-Volatile cache: Cache that retains data through all power and reset events. Non-volatile cache shall be a subset of the non-volatile media.~~

3.1.39 Nexus Loss Event: TBD

Editor's Note 5: AAM: 3.1.23 nexus loss event: a transport specific event where the host port is no longer in communication with a device port (e.g., a device was removed from a computer system). This needs further work to correlate to unrecovered loss of PHYRDY.

3.1.40 ~~Non-Volatile Media:~~ ~~Physical storage media that retains data written to it for subsequent read operations through all power and reset events (e.g., magnetic media, optical media, flash media).~~

3.1.41 ~~NV Cache Pinned Set:~~ ~~The set of logical blocks that have been made un-removable from the NV Cache by the host. Writes to logical blocks represented in the NV Cache Pinned Set always results in valid data in the NV Cache Set.~~

3.1.42 ~~NV Cache Set:~~ ~~The set of logical blocks currently represented in the device's entire NV Cache.~~

3.1.43 ~~NV Cache Set Data:~~ ~~A data structure representing the standard format of transmitting logical blocks in the form of a list of LBA Range Entries.~~

3.1.44 ~~NV Cache Unpinned Set:~~ ~~The set of logical blocks that are represented in the NV Cache Set but not represented in the NV Cache Pinned Set. The NV Cache Pinned Set and the NV Cache Unpinned Set are mutually exclusive. NV Cache Unpinned Set is completely managed by the device and logical blocks represented in the NV Cache Unpinned Set may be added or removed from the NV Cache Set at any time.~~

3.1.45 ~~Password Attempt Counter Exceeded:~~ ~~There were too many attempts to unlock the device with an incorrect password. This is a name associated with IDENTIFY DEVICE, word 128, bit 4.~~

3.1.46 ~~PATA:~~ ~~A device implementing the parallel transport, see ATA8-APT~~

3.1.47 ~~physical sector:~~ ~~One or more contiguous logical sectors that are read from or written to the device media in a single operation.~~

3.1.48 PIO (programmed input/output) data transfer: PIO data transfers are performed using PIO commands and protocol.

3.1.49 power cycle: the period from when power is removed from a host or device until the subsequent power-on event (see ATA8-AAM).

3.1.50 power-on reset: the host specific routine performed by the host or the routine performed by a device after detecting a power-on event. The power-on reset routine performed by a device includes the actions performed by the device for a hardware reset and a software reset, and the actions defined in ATA8-AAM, this standard, and the applicable transport standards.

3.1.51 queued: Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the Tagged Command Queuing (TCQ) feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred but command completion has not occurred.

3.1.52 Queued Command: A NCQ command that has reported command acceptance but not command completion.

3.1.53 Word: A sequence of eight contiguous bytes considered as a unit. See 3.3.8.

3.1.54 RDH FIS: Register - Device to Host FIS. See SATA-2.6 and SATA-3.0

3.1.55 RHD FIS: Register - Host to Device FIS. See SATA-2.6 and SATA-3.0

3.1.56 read command: A command that causes the device to transfer data from the device to the host. The following commands are read commands: READ DMA, READ DMA EXT, READ DMA QUEUED, READ DMA QUEUED EXT, READ FPDMA QUEUED, READ MULTIPLE, READ MULTIPLE EXT, READ SECTOR(S), READ SECTOR(S) EXT, READ STREAM DMA, READ STREAM DMA EXT, READ VERIFY SECTOR(S), or READ VERIFY SECTOR(S) EXT.

3.1.57 release: The action by a device implementing the TCQ feature set that allows a host to select an alternate device or deliver another queued command.

3.1.58 SATA: A device implementing the serial transport, see ATA8-AST

3.1.59 sector: See logical sector.

3.1.60 ~~Security Is Disabled:~~ ~~The Security feature set is supported, but there is no valid User password. There is a Master password. Access to user data is not restricted by the Security feature set. The terms 'Security Is Locked' and 'Security Is Unlocked' are not applicable. (e.g., Security states SEC0, SEC1, SEC2).~~

3.1.61 ~~Security Is Enabled:~~ ~~The Security feature set is supported, and a valid User password has been set. (e.g., Security states SEC3, SEC4, SEC5, SEC6).~~

3.1.62 ~~Security Is Frozen:~~ ~~Security may be either enabled or disabled. Changes to Security states are not allowed until after the next power on or hardware reset. (e.g., Security states SEC2, SEC6).~~

3.1.63 ~~Security Is Locked:~~ ~~Security is enabled. In addition, access to the device is restricted. (e.g., Security state SEC4).~~

3.1.64 ~~Security Is Not Frozen:~~ ~~Security may be either enabled or disabled. Changes to Security states are allowed (e.g., Security states SEC1, SEC4, SEC5).~~

3.1.65 ~~Security Is Unlocked: Security is enabled.~~ ~~A SECURITY UNLOCK command was successful, allowing access to the device. (e.g., Security state SEC5, SEC6).~~

3.1.66 ~~Security Level:~~ ~~See Master Password Capability.~~

3.1.67 signature: A unique set of values placed in the return parameters used to distinguish command sets (e.g., General, ATAPI device, Port Multiplier).

3.1.68 software reset: the routine performed by a device after a software reset event as defined in ATA8-AAM. The software reset routine includes the actions defined in ATA8-AAM, this standard, and the applicable transport standards.

3.1.69 ~~spin-down:~~ ~~the process of bringing a rotating media device's media to a stop.~~

3.1.70 ~~spin-up:~~ ~~the process of bringing a rotating media device's media to operational speed.~~

3.1.71 ~~Spindle State:~~ ~~The current state of the device's rotational media. There are two possible states: spun up/spinning up and spun down/spinning down.~~

3.1.72 Stream: a set of operating parameters specified by a host using the CONFIGURE STREAM command to be used for subsequent READ STREAM commands and WRITE STREAM commands.

3.1.73 ~~TCG: Trusted Computing Group:~~ ~~An organization that develops and promotes open standards for hardware-enabled trusted computing and security technologies. See taps://www.trustedcomputing-group.org for more information.~~

3.1.74 ~~TCQ (Tagged Command Queuing):~~ ~~TCQ feature set.~~

3.1.75 transport: a mechanism used to communicate between a host and a device.

3.1.76 ~~unaligned write:~~ ~~A write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector.~~

3.1.77 ~~unrecoverable error:~~ ~~When the device sets either the ERR bit or the DF bit to one in the Status field at command completion.~~

3.1.78 ~~Volatile Cache:~~ ~~Cache that does not retain data through power cycles.~~

3.1.79 ~~VS (vendor specific):~~ ~~Bits, bytes, fields, and code values that are reserved for vendor specific purposes. These bits, bytes, fields, and code values are not described in this standard, and implementations may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.~~

3.1.80 word: A sequence of two contiguous bytes considered as a unit. See 3.3.8.

3.1.81 write command: A command that causes the device to transfer data from the host to the device. The following commands are write commands: WRITE DMA, WRITE DMA EXT, WRITE DMA FUA EXT, WRITE DMA QUEUED, WRITE DMA QUEUED EXT, WRITE DMA QUEUED FUA EXT, WRITE FPDMA QUEUED, WRITE MULTIPLE, WRITE MULTIPLE EXT, WRITE MULTIPLE FUA EXT, WRITE SECTOR(S), WRITE SECTOR(S) EXT, WRITE STREAM DMA EXT, or WRITE STREAM EXT.

3.1.82 ~~WWN (world wide name):~~ ~~A 64-bit worldwide unique name based upon a company's IEEE organizationally unique identifier (OUI), reported in IDENTIFY DEVICE data words 108-111 and IDENTIFY PACKET DEVICE data words 108-111~~

3.2 Symbols and abbreviations

Abbreviation	Meaning
FIS	Frame Information Structure
RDH FIS	Register Device to Host FIS
RHD FIS	Register Host to Device FIS
SDB FIS	Set Device Bits FIS

3.3 Conventions

3.3.1 Overview

Lowercase is used for words having the normal English language meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English language meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the “name” bit instead of the “name” field. (See 3.3.6 for the naming convention used for naming bits.)

Names of device fields begin with a capital letter (e.g., Count).

The expression “word n” or “bit n” shall be interpreted as indicating the content of word n or bit n.

3.3.2 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, then text.

3.3.3 Lists

Unordered lists, those lists describing a sequence, are of the form:

a)
b)
c)

Ordered list are of the form:

1)
2)
3)

3.3.4 Keywords

Several keywords are used to differentiate between different levels of requirements and options.

3.3.4.1 expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.3.4.2 mandatory: A keyword indicating items to be implemented as defined by this standard.

3.3.4.3 may: A keyword that indicates flexibility of choice with no implied preference.

3.3.4.4 N/A: A keyword that indicates a field is not applicable and has no defined value and should not be checked by the host or device.

3.3.4.5 obsolete: A keyword indicating that the designated bits, bytes, words, fields, and code values that may have been defined in previous standards are not defined in this standard and shall not be reclaimed for other uses in future standards. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility.

Obsolete commands should not be used by the host. Commands defined as obsolete may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

3.3.4.6 optional: A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

3.3.4.7 prohibited: A keyword indicating that an item shall not be implemented by an implementation.

3.3.4.8 reserved: A keyword indicating reserved bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

3.3.4.9 retired: A keyword indicating that the designated bits, bytes, words, fields, and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, words, fields, or code values are used before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

3.3.4.10 shall: A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.3.4.11 should: A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

3.3.5 Numbering

Numbers that are not immediately followed by a lowercase “b” or “h” are decimal values. Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) are hexadecimal values.

3.3.6 Bit conventions

Bit (n:m) denotes a set of bits, for example, bits (7:0).

3.3.7 State diagram conventions

State diagrams shall be as shown in Figure 2.

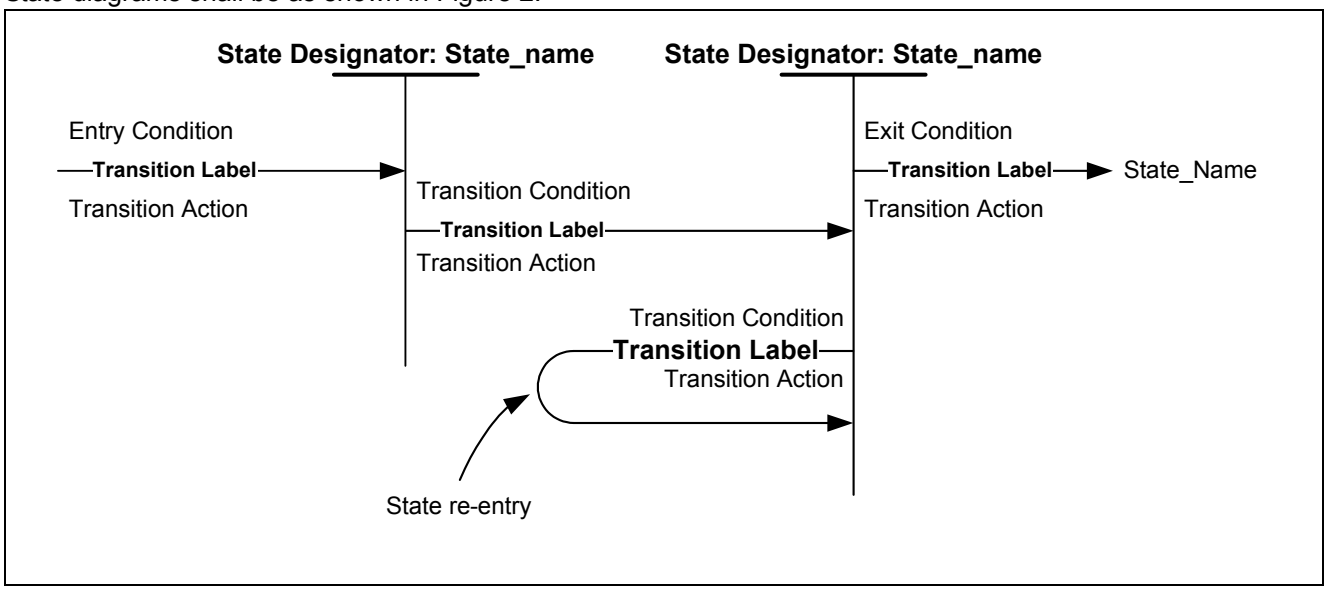


Figure 2 — State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state, and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled State_name. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

Transitions from state to state shall be instantaneous.

3.3.8 Byte, word, DWord, and QWord Relationships

Figure 3 illustrates the relationship between bytes, words DWords, and QWords.

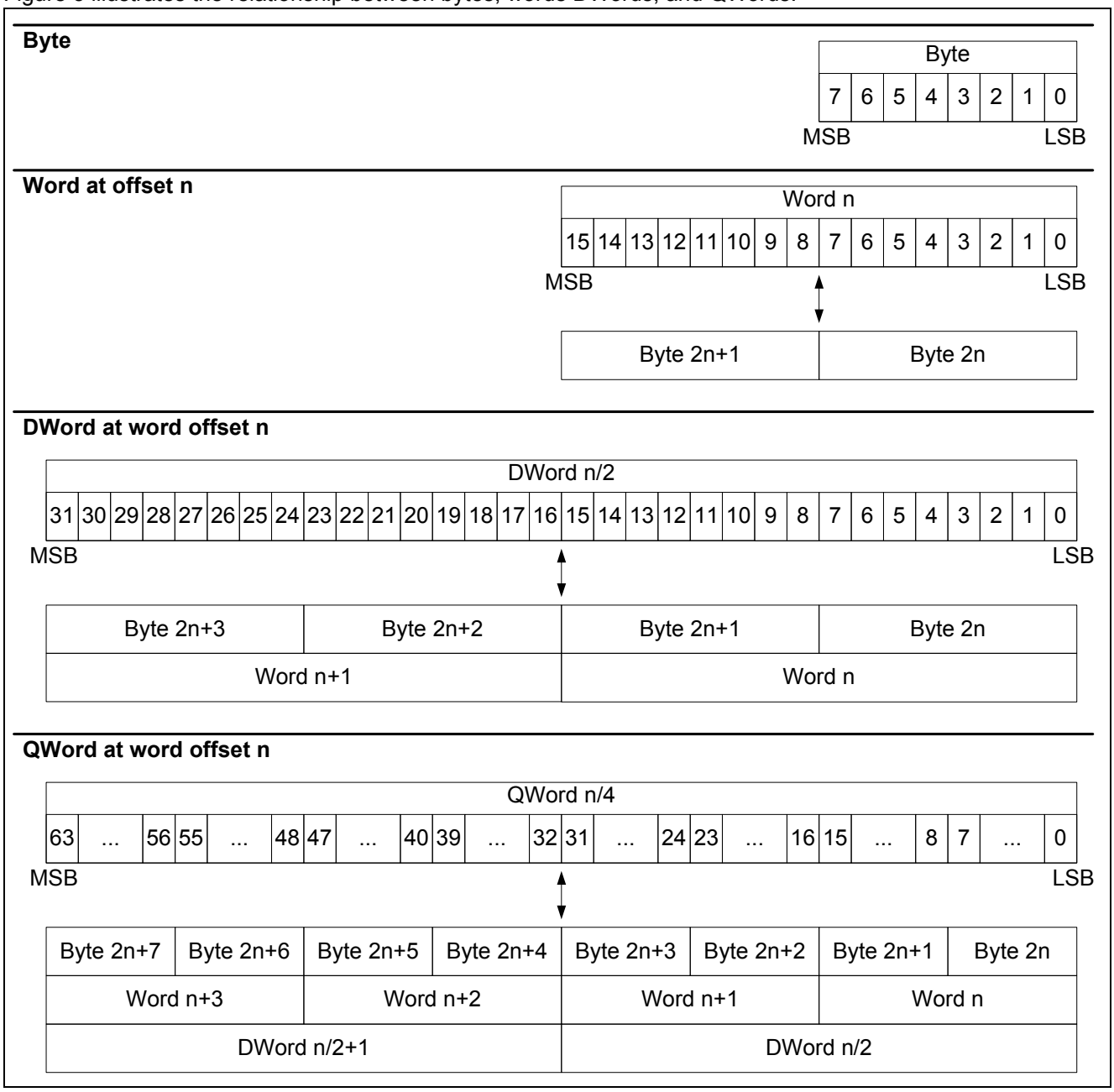


Figure 3 — Byte, word, Word and QWord relationships

Unless stated or defined otherwise, in a field containing a multi-byte value (e.g., a word, DWord, or QWord), the byte containing the LSB is stored at the lowest offset and the byte containing the MSB is stored at the highest offset. Examples following this convention include:

a) Device Configuration Identify data;
b) IDENTIFY DEVICE data;
c) IDENTIFY PACKET DEVICE data;
d) Request Pin data, Cache Miss Data, Pin Set Data, and Remove Pin Data used by Non-Volatile Cache commands;
e) Device SMART data;
f) SCT status response and SCT command; and
g) Logs;

For example if an eight-byte field (i.e., QWord) in the WRITE SAME command words 2-5 contains 0000_0504_0302_0100h), then:

a) byte 4 contains 00h;
b) byte 5 contains 01h;
c) byte 6 contains 02h;
d) byte 7 contains 03h;
e) byte 8 contains 04h;
f) byte 9 contains 05h;
g) byte 10 contains 00h; and
h) byte 11 contains 00h;

Exceptions to this convention include:

a) each field containing an ATA string (e.g., the IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data Serial number, Firmware revision, and Model number fields) is considered to be an array of bytes, not a multi-byte value, and is handled as described in 3.3.9;
b) the IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data World Wide Name field is treated as four word fields rather than one QWord field; and
c) the CFA TRANSLATE SECTOR data LBA and logical sector write cycles count fields;
d) the command packet in the PACKET command is formatted as defined by the applicable command standard); and
e) parameter data in the TRUSTED RECEIVE, TRUSTED RECEIVE DMA, TRUSTED SEND, and TRUSTED SEND DMA commands is formatted as defined in those sections or in the standard defining the security protocol.

3.3.9 ATA string convention

ATA strings are sequences of bytes containing ASCII graphic characters in the range of 20h-7Eh. ATA strings shall not contain values in the range of 00h-1Fh or 7Fh-FFh.

Three fields in IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data contain ATA strings:

a) Serial number (words 10-19);
b) Firmware revision (words 23-26);
c) Model number (words 27-46); and
d) Current media serial number (words 176-205).

However, these ATA strings are not stored in the normal ASCII string format where byte offset 0 contains the first character, byte offset 1 contains the second character, etc. Each pair of bytes in ATA strings is swapped as shown in table 3.

Table 3 — ATA string byte swapping

Word	Byte	Character in string
0	0	Second character
	1	First character
1	2	Fourth character
	3	Third character
...	...	...
n	2n	Last character
	2n+1	Second-to-last character

For example, if the Firmware revision number field (words 23-26) contains the string “abcdefg ” (including one padding space character at the end), its word and byte representations are shown in table 4.

Table 4 — ATA firmware revision example

Word	Value	Byte	Value
23	6162h (i.e., “ba”)	46	62h (i.e., “b’)
		47	61h (i.e., “a”)
24	6364h (i.e., “dc”)	48	64h (i.e., “d”)
		49	63h (i.e., “c”)
25	6566h (i.e., “fe”)	50	66h (i.e., “f”)
		51	65h (i.e., “e”)
26	6720h (i.e., “ g”)	52	20h (i.e., “ “, the space character)
		53	67h (i.e., “g”)

4 Mapping AAM and ACS-2 to AST

Editor's Note 6: From AAM
AT Attachment-8 Serial Transport (ATA8-AST): defines the following for the serial ATA interface:
a) the connectors and cables for physical interconnection between host and storage device;
b) the electrical characteristics of the interconnecting signals;
c) the logical characteristics of the interconnecting signals; and
d) the protocols for transporting commands, data, and status using the interface.

4.1 Mapping Overview

Editor's Note 7: Section 4.1 is under development

4.2 Mapping ACS-2 and SATA-2.6 fields

4.2.1 Mapping ACS-2 command fields into SATA-2.6 RHD FIS fields

The Register Host to Device Frame Information Structure (RHD FIS) is a transport specific mechanism to pass ACS defined commands (see ACS-2) from a host to a SATA device in a SATA-IO defined structure (see SATA 2.6 and SATA 3.0).

The mapping of ACS 28-bit command fields to RHD FIS fields is described in table 5. The mapping of ACS 48-bit command fields to RHD FIS fields is described in table 6..

Table 5 — 28-Bit Command Mapping

ACS FIeld	FIS Field
Feature (7:0)	Feature
Count (7:0)	Sector Count
LBA (7:0)	LBA Low
LBA (15:8)	LBA Mid
LBA (23:16)	LBA High
LBA (27:24)	Device (3:0)
Device (15:12)	Device (7:4)
Command	Command
Note 1 - SATA RHD FIS Fields Feature (exp), Sector Count (exp), LBA Low (exp), LBA Mid (exp), LBA High (exp) are not used in 28-bit commands	

Table 6 — 48-Bit Command Mapping

ACS FIeld	FIS Field
Feature (7:0)	Feature
Feature (15:8)	Feature (exp)
Count (7:0)	Sector Count
Count (15:8)	Sector Count (exp)
LBA (7:0)	LBA Low
LBA (15:8)	LBA Mid
LBA (23:16)	LBA High
LBA (31:24)	LBA Low (exp)
LBA (39:32)	LBA Mid (exp)
LBA (47:40)	LBA High (exp)
Device (15:12)	Device (7:4)
Command	Command
Note 1 - SATA RHD FIS Field Device (3:0) is not used in 28-bit commands	

4.2.2 Mapping ACS-2 Normal Outputs and Error Outputs into a RDH FIS

The Register Device to Host Frame Information Structure (RDH FIS) is a transport specific mechanism to pass ACS defined Normal outputs nd Error outputs (see ACS-2) from a SATA device to a host in a SATA-IO defined structure (see SATA 2.6 and SATA 3.0).

The mapping of ACS 28-bit Normal output and Error output fields to RDH FIS fields is described in table 7. The mapping of ACS 48-bit Normal output and Error output fields to RDH FIS fields is described in table 8..

Table 7 — 28-Bit Normal/Error Mapping

ACS-2 FIeld	FIS Field
Error (7:0)	Error
Count (7:0)	Sector Count
LBA (7:0)	LBA Low
LBA (15:8)	LBA Mid
LBA (23:16)	LBA High
LBA (27:24)	Device (3:0)
Device (15:12)	Device (7:4)
Status	Status
Note - SATA RDH FIS Fields Sector Count (exp), LBA Low (exp), LBA Mid (exp), LBA High (exp) are not used in 28-bit commands	

Table 8 — 48-Bit Normal/Error Mapping

ACS Field	FIS Field
Error (7:0)	Error
Count (7:0)	Sector Count
Count (15:8)	Sector Count (exp)
LBA (7:0)	LBA Low
LBA (15:8)	LBA Mid
LBA (23:16)	LBA High
LBA (31:24)	LBA Low (exp)
LBA (39:32)	LBA Mid (exp)
LBA (47:40)	LBA High (exp)
Device (15:12)	Device (7:4)
Command	Command
~~Note 1 –~~	

4.2.3 Mapping ACS-2 Normal Outputs and Error Outputs into a SDB FIS

The Set DeviceBits Frame Information Structure (SDB FIS) is a transport specific mechanism to pass ACS defined device information (see ACS-2) to a host in a SATA-IO defined structure (see SATA 2.6 and SATA 3.0). The mapping of ACS fields to SDB FIS fields is described in table 9.

Table 9 — 48-Bit Queue Aborted Mapping

ACS Field	FIS Field
Error (15:8)	Error
Status (7:0)	Status
SActive (31:0)	Sactive

4.3 AST specific ACS-2 Transport Dependent responses

Editor's Note 8: Section 4.3 will be developed in a new seperate proposal

Command Completion (4.17.4.3)	See SDB FIS
Busy bit (6.2.3)	
Data Request bit (6.2.5)	
Device Ready Bit (6.2.8)	
Normal Output Device field bit 4 (7.1.5)	
Normal Output Status field bit 7 (7.1.5)	
Normal Output Device field bit 6 (7.1.5)	
Error Output Device field bit 4 (7.1.6)	
Error Output Status field bit 7 (7.1.6)	

Error Output Device field bit 6 (7.1.6)	
Error Output Device field bit 3 (7.1.6)	
Device Signatures for Normal Outputs	
NCQ Normal Output SATA Status (Table 116)	
NCQ Read Command Aborted Output SATA Status (Table 156)	

4.4 Mapping of Identify Device and Identify Packet Device

Editor's Note 9: Requirement for this section are in development

Identify Device Command

	<Editor's Note: Compare to SATA for interesting descripencies>
7.18.7.15 Word 47	For SATA devices, bits (7:0) shall be set to 16 or less.
7.18.7.17 Words 49..50: Capabilities	For SATA devices, bit 11 of word 49 shall be set to one. For SATA devices, bit 10 of word 49 shall be set to one.
7.18.7.19 Word 53	For SATA devices, bit 2 of word 53 shall be set to one. For SATA devices, bit 1 of word 53 shall be set to one.
7.18.7.24 Word 63 Multiword DMA transfer modes	For SATA devices, bit 2 of word 63 shall be set to one. For SATA devices, bit 1 of word 63 shall be set to one. For SATA devices, bit 0 of word 63 shall be set to one.
7.18.7.25 Word 64 PIO data and register transfer supported field.	For SATA devices bits (1:0) shall be set to one
7.18.7.26 Word 65: Minimum Multiword DMA transfer cycle time per word	For SATA devices word 65 shall be set to indicate 120 nanoseconds
7.18.7.27 Word 66: Device recommended Multiword DMA transfer cycle time	For SATA devices, word 66 shall be set to 78h to indicate 120 nanoseconds.
7.18.7.28 Word 67: Minimum PIO transfer cycle time without IORDY flow control	For SATA devices word 67 shall be set to indicate 120ns.
7.18.7.29 Word 68: Minimum PIO transfer cycle time with IORDY flow control.	For SATA devices word 68 shall be set to indicate 120ns.

<Editor's Note: Compare to SATA for interesting descripencies>

7.18.7.34 Word 76: Serial ATA Capabilities	Bits (15:13) of word 76 are reserved for Serial ATA. If bit 12 of word 76 is set to one, then the device supports the Priority field in the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands and optimization based on this information. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76. If bit 11 of word 76 is set to one, then the device supports performing an unload/park of the heads upon reception of the IDLE IMMEDIATE command with the Unload Feature specified while NCQ commands are outstanding. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76. If bit 10 of word 76 is set to one, then the device supports the SATA Phy Event Counters log (see A.14). If bit 9 of word 76 is set to one, then the device supports Partial and Slumber interface power management states when initiated by the host (see SATA 2.6). If bit 8 of word 76 is set to one, then the device supports the NCQ feature set. Bits (7:3) of word 76 are reserved for Serial ATA. If bit 2 of word 76 is set to one, then the device supports the Gen2 signaling rate of 3.0 Gb/s (see SATA 2.6). If bit 1 of word 76 is set to one, then the device supports the Gen1 signaling rate of 1.5 Gb/s (see SATA 2.6). Bit 0 of word 76 shall be cleared to zero.
7.18.7.35 Word 77: Reserved for Serial ATA	Word 77 is reserved for future Serial ATA definition and shall be cleared to zero
7.18.7.36 Word 78: Serial ATA features supported	Bits (15:7) are reserved for Serial ATA. If bit 6 is set to one, then the device supports the SSP feature set (see 4.25). Bit 5 is reserved for Serial ATA. If bit 4 is set to one the device supports guaranteed in-order data delivery when non-zero buffer offsets are used for commands in the NCQ feature set. See SATA 2.6 for more information. If bit 3 is set to one the device supports device initiated power management requests. If bit 3 is cleared to zero the device does not support device initiated power management requests. A device may support reception of power management requests initiated by the host as described in the definition of bit 9 of Word 76 without supporting initiating such power management requests as indicated by this bit. If bit 2 is set to one the device supports the use of the DMA Setup FIS Auto-Activate optimization. See SATA 2.6 for more information. If bit 1 is set to one the device supports the use of non-zero buffer offsets for commands in the NCQ feature set. See SATA 2.6 for more information. Bit 0 shall be cleared to zero.

<Editor's Note: Compare to SATA for interesting descripencies>

7.18.7.37 Word 79: Serial ATA features enabled	Bits (15:7) are reserved for Serial ATA. If bit 6 is set to one then the SSP feature set is enabled. If the device supports the SSP feature set, then this field shall be one after a power on reset has been processed. If the device does not support the SSP feature set, then this field shall be zero by default. Bit 5 is reserved for Serial ATA. If bit 4 is set to one then device support for guaranteed in-order data delivery when non-zero buffer offsets are used for commands in the NCQ feature set is enabled. See SATA 2.6 for more information. If bit 3 is set to one then device support for initiating power management requests to the host is enabled. When set to one the device may initiate power management transition requests. When cleared to zero the device shall not initiate interface power management requests to the host. This field shall be zero by default. If bit 2 is set to one then the device support for use of the DMA Setup FIS Auto-Activate optimization is enabled. See SATA 2.6 for more information. If bit 1 is set to one then device support for the use of non-zero buffer offsets for commands in the NCQ feature set is enabled. See SATA 2.6 for more information. Bit 0 shall be cleared to zero.
7.18.7.42 Word 88: Ultra DMA modes	For SATA devices bit 6 of word 88 shall be set to one. For SATA devices bit 5 of word 88 shall be set to one. For SATA devices bit 4 of word 88 shall be set to one. For SATA devices bit 3 of word 88 shall be set to one. For SATA devices bit 2 of word 88 shall be set to one. For SATA devices bit 1 of word 88 shall be set to one. For SATA devices bit 0 of word 88 shall be set to one.
7.18.7.47 Word 93: Hardware reset results	For SATA devices, word 93 shall be set to the value 0000h.
7.18.7.86 Word 222: Transport major version number	Transport major version number (see 7.18.7.86) 0000h or FFFFh = device does not report version 15:12 Transport Type 1h = Serial 11:6 Reserved Reserved A device may set more than one of the following bits to one. 5 SATA Rev 3.0 4 SATA Rev 2.6 3 SATA Rev 2.5 2 SATA II: Extensions 1 SATA 1.0a 0 ATA8-AST

Identyify Packet Device Command

7.19.6.10 Word 47	Reserved
7.19.6.11 Words 49..50: Capabilities	For SATA devices, bit 11 of word 49 shall be set to one. For SATA devices, bit 10 of word 49 shall be set to one.
7.19.6.15 Word 53	For SATA devices, bit 2 of word 53 shall be set to one. For SATA devices, bit 1 of word 53 shall be set to one.

	For SATA devices, bit 2 of word 63 shall be set to one except this bit shall be cleared to zero for Serial ATAPI devices requiring the DMADIR bit in the PACKET command.
7.19.6.18 Word 63 Multiword DMA transfer modes	For SATA devices, bit 1 of word 63 bit shall be set to one except this bit shall be cleared to zero for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices, bit 0 of word 63 shall be set to one except this bit shall be cleared to zero for Serial ATAPI devices that require the DMADIR bit in the PACKET command.
7.19.6.19 Word 64 PIO data and register transfer supported field.	For SATA devices bits (1:0) shall be set to one
7.19.6.20 Word 65: Minimum Multiword DMA transfer cycle time per word	For SATA devices word 65 shall be set to indicate 120 nanoseconds
7.19.6.21 Word 66: Device recommended Multiword DMA transfer cycle time	For SATA devices, word 66 shall be set to 78h to indicate 120 nanoseconds.
7.19.6.22 Word 67: Minimum PIO transfer cycle time without IORDY flow control	For SATA devices word 67 shall be set to indicate 120ns.
7.19.6.23 Word 68: Minimum PIO transfer cycle time with IORDY flow control.	For SATA devices word 68 shall be set to indicate 120ns.
7.19.6.28 Word 76: Serial ATA Capabilities	Bits (15:13) of word 76 are reserved for Serial ATA. If bit 12 of word 76 is set to one, then the device supports the Priority field in the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands and optimization based on this information. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76. If bit 11 of word 76 is set to one, then the device supports performing an unload/park of the heads upon reception of the IDLE IMMEDIATE command with the Unload Feature specified while NCQ commands are outstanding. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76. If bit 10 of word 76 is set to one, then the device supports the SATA Phy Event Counters log (see A.14). If bit 9 of word 76 is set to one, then the device supports Partial and Slumber interface power management states when initiated by the host (see SATA 2.6). If bit 8 of word 76 is set to one, then the device supports the NCQ feature set. Bits (7:3) of word 76 are reserved for Serial ATA. If bit 2 of word 76 is set to one, then the device supports the Gen2 signaling rate of 3.0 Gb/s (see SATA 2.6). If bit 1 of word 76 is set to one, then the device supports the Gen1 signaling rate of 1.5 Gb/s (see SATA 2.6). Bit 0 of word 76 shall be cleared to zero.
7.19.6.29 Word 77: Reserved for Serial ATA	Word 77 is reserved for future Serial ATA definition and shall be cleared to zero

7.19.6.30 Word 78: Serial ATA features supported	Bits (15:7) are reserved for Serial ATA. If bit 6 is set to one, then the device supports the SSP feature set (see 4.25). Bit 5 is reserved for Serial ATA. If bit 4 is set to one the device supports guaranteed in-order data delivery when non-zero buffer offsets are used for commands in the NCQ feature set. See SATA 2.6 for more information. If bit 3 is set to one the device supports device initiated power management requests. If bit 3 is cleared to zero the device does not support device initiated power management requests. A device may support reception of power management requests initiated by the host as described in the definition of bit 9 of Word 76 without supporting initiating such power management requests as indicated by this bit. If bit 2 is set to one the device supports the use of the DMA Setup FIS Auto-Activate optimization. See SATA 2.6 for more information. If bit 1 is set to one the device supports the use of non-zero buffer offsets for commands in the NCQ feature set. See SATA 2.6 for more information. Bit 0 shall be cleared to zero.
7.19.6.31 Word 79: Serial ATA features enabled	Bits (15:7) are reserved for Serial ATA. If bit 6 is set to one then the SSP feature set is enabled. If the device supports the SSP feature set, then this field shall be one after a power on reset has been processed. If the device does not support the SSP feature set, then this field shall be zero by default. Bit 5 is reserved for Serial ATA. If bit 4 is set to one then device support for guaranteed in-order data delivery when non-zero buffer offsets are used for commands in the NCQ feature set is enabled. See SATA 2.6 for more information. If bit 3 is set to one then device support for initiating power management requests to the host is enabled. When set to one the device may initiate power management transition requests. When cleared to zero the device shall not initiate interface power management requests to the host. This field shall be zero by default. If bit 2 is set to one then the device support for use of the DMA Setup FIS Auto-Activate optimization is enabled. See SATA 2.6 for more information. If bit 1 is set to one then device support for the use of non-zero buffer offsets for commands in the NCQ feature set is enabled. See SATA 2.6 for more information. Bit 0 shall be cleared to zero.

7.19.6.36 Word 88: Ultra DMA modes	For SATA devices bit 6 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 5 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 4 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 3 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 2 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 1 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command. For SATA devices bit 0 of word 88 shall be set to one except for Serial ATAPI devices that require the DMADIR bit in the PACKET command.
7.19.6.41 Word 93: Hardware reset results	For SATA devices, word 93 shall be set to the value 0000h.
7.19.6.55 Word 222: Transport major version number	Transport major version number (see 7.18.7.86) 0000h or FFFFh = device does not report version 15:12 Transport Type 1h = Serial 11:6 Reserved Reserved A device may set more than one of the following bits to one. 5 SATA Rev 3.0 4 SATA Rev 2.6 3 SATA Rev 2.5 2 SATA II: Extensions 1 SATA 1.0a 0 ATA8-AST

4.5 AAM Protocols

Editor's Note 10: Section 4.5 will be developed in a new seperate proposal

4.5.1 Native Command Queuing

The Native Command Queuing model is a DMA model defined by SATA-IO (see SATA 2.6 and SATA 3.0).

The Native Command Queued commands are defined by T10 (see ACS-2).

Hard Reset: A Send Management Function Request (see AAM) is implemented as COMRESET, a signal event defined by SATA-IO (see SATA 2.6 and SATA 3.0)

Annex A
(Normative)

Place Holder Annex

A.1 Overview

Place Holder.

Table A.1 — Sample Table
