

Accredited Standards Committee*
NCITS, National Committee for Information Technology Standards

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Reply to: Lawrence J. Lamers

To: Membership of T13
From: Lawrence J. Lamers, Secretary T13
Gene Milligan, Chair T13
Subject: Minutes of T13 Working Group
May 21-23, 1997 : Estes Park, CO

Agenda

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Results of Meeting

1. Opening Remarks

Gene Milligan called the meeting to order at 9:00 a.m., Wednesday May 21, 1997. He thanked Marc Noblitt of Seagate Technology for hosting the meeting.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by T13 and would be conducted under the T13 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the Technical Committee. The voting rules for the meeting are those of the parent committee, T13. For the ad hoc, other than straw votes, the voting rules are: one vote per participating organization.

Gene Milligan informed the attendees that, as Chair of T13, he preferred to be a "Non-voting Chair" with another Seagate employee Marc Noblitt functioning as the voting member. He indicated the motivation was to facilitate an attempt to Chair the meetings without bias to a specific faction's position. However, even in this mode he would reserve the right to cast a vote in the event there were no Seagate representatives present.

The minutes of this meeting will be posted to the T13 ftp site and the T13 Reflector and will be included in the next T13 committee mailing.

2. Approval of Agenda

The electronically distributed agenda was used as a basis for the meeting with adjustments as reflected in these minutes.

3. Attendance

Attendance at working group meetings does not count toward minimum attendance requirements for membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

Wen	Lin	Adaptec	G
Lawrence	Lamers	Adaptec, Inc.	A1
Martin	Soques	Advanced Micro Devices	G
Hale	Landis	Consultant	P
Steve	Hartung	Exabyte Corp.	G
Tony	Goodfellow	GSI	P
Anthony	Yang	Hitachi America Ltd.	P
Dan	Colegrove	IBM Corp.	P
Terry	Miller	Iomega Corp.	G
Pete	McLean	Maxtor Corp.	P
Lance	Flake	O.R. Technology	P
Christopher	Mayne	O.R. Technology	A
Mike	Christensen	Phoenix Technologies	A
Mark	Evans	Quantum Corp.	P
Yasuyuki	Suemori	Sanyo Electric Co., Ltd.	A
Gene	Milligan	Seagate Technology	P
Marc	Noblitt	Seagate Technology	A
Paresh	Sheth	Silicon Systems, Inc.	P
Yogi	Schaffner	Silicon Systems, Inc.	A
Jeff	Cousins	SyQuest Technology	G
Tokuyuki	Totani	Toshiba America Info.	P
Tom	Hanan	Western Digital Corp.	P
Jonathan	Hanmann	Western Digital Corp.	G

4. Document Distribution

The following documents were distributed:

- T13 Document Register - 1997
- T13/1153D Rev 12 ATA/ATAPI-4 [McLean]
- T13/1226 DT Rev 3 EDD [Stevens]
- D97121R0 80 Conductor Cable
- D97134r0 PIO Response Table
- D97135r0 Proposal for Solution to the command queuing Set Interrupt Race
- D97137r0 SRST protocol for overlapped and queued devices
- D97120R1 Removable Media Feature Set
- D97119R2 SET MAX calculations
- D97126r1 Proposed APM feature

5. Review of Old Action Items

76) Tom Hanan to develop a proposal for error register use on packet devices. Completed.

6. ATA/ATAPI-4 - Project 1153D**6.1 Review of working draft**

Pete McLean stated that rev 12 is available. Pete conducted a review of the flow diagrams and change bars.

Add a reference to 7.15.6.1 to setting of BSY in the flow charts.

Add recommendation for host to read status or alternate status register at end of PIO transfer (Fig 10).

Fig 13 should DRQ be set during the transfer? Add box to allow setting DRQ as an option.

Fig 14 - should DRDY and DSC be set for compatibility with old drivers when DRQ is set.

Tom Hanan stated that the only way to clear a SERV bit for a command is for the host to issue a SERVICE command with the tag for that command. The device asserts INTRQ for the service request until the command is completed by the host reading the status register of the SERVICE command. INTRQ may remain asserted if there are back to back service requests.

Device completes a command and interrupts. The device at this time has another command ready for service.

- 1) The SERV bit will be set in the STATUS register for the command just completed.
- 2) After command completion the interrupt is cleared the device shall interrupt again for service.

INTRQ may remain asserted if there are back to back service requests.

Change host read of status or alternate status to read of status to ensure that an internal pending interrupt is cleared.

6.2 Set Max [Colegrove] (D97119)

Dan Colegrove reviewed revision 2. Additional changes were made. Phoenix Technologies stated that they plan to use and implement this feature so it will stay in D1153.

6.3 Annex C changes from Ultra DMA (D97128)

Mark Evans plans to complete this proposal in the near future.

6.4 Reset(s) Impact on Features Register [] (D97)

The current draft is silent on what happens to the Features Register when a reset occurs. The consensus is that the effect of reset on the feature register should be undefined.

6.5 Reset(s) Impact on Execute Device Diagnostics[] (D97)

The consensus is that the effect of reset on the feature register following an Execute Device Diagnostics should be undefined.

6.6 Command Completes vis a vis Immediate Commands, Write Caching, and Executing [Landis] (D97)

In 9.1.2/3 steps 4b and 5b change “..but shall not interrupt..” to “..”and the device is not expected to stop any background device activity (e.g. immediate commands, see MMC) that was started prior to the time that SRST was set to one in step 1)”.

Add also to 9.4 setup 4 a statement that “The device is expected to end background activity (e.g., immediate commands, see MMC).

6.7 INTRQ Biasing [] (D97)

An issue was pointed out that if a host uses level sensitive interrupts a 10k pull up is needed since if both devices release the bus the signal will float. In a properly implemented system this float can only occur during the 400 ns period that occurs when switching devices so it should be ignored and not be a problem.

6.8 Interrupt Race [Schaffner] (D97135)

There are two asynchronous events occurring; to get predictable behavior Yogi proposed that the events have to be resolved by some method of discrete clocking.

The races are:

- 1) The host writes the command register as the device is setting SERV and INTRQ. (happens with queuing)
 - 2) The host reads status register as the device is setting SERV and INTRQ. (happens with queuing)
 - 3) The host writes the drive/head register to select the other device as the device is setting SERV and INTRQ. (happens with queuing or overlap)
 - 4) The host writes nIEN as the device is setting the INTRQ. (happens with or without queuing/overlap)
- The race condition occurs in the interrupt controller.

The solutions are:

- 1) The SERV bit is set as soon as device has a queued command ready to be serviced regardless of other command activity. The host should disable the interrupts using nIEN before writing the command register in a queued environment.
- 2) The host should not read the status register while an interrupt is expected.
- 3) Require the host to disable interrupts in a separate bus cycle before selecting the other device.
- 4) When interrupts are being disabled using nIEN, if the device asserts INTRQ the minimum width pulse shall be 340 ns, or until status register is read, or command register written.

There was consensus that these solutions are adequate.

6.9 Error Register Bits for Packet Commands [Hanan] (D97)

The error register was changed to n/a.

6.10 DSC/SERV Bit [] (D97)

The DSC/SERV bit is command set specific. The only place where the two meanings exist is in the PACKET COMMAND. If overlap enabled the bit is defined as SERV, otherwise it is command specific.

A note will be added to the register clause indicating prior usage as DSC.

6.11 SRST protocol for overlapped and queued devices [Hanan] (D97137)

Tom Hanan presented a proposal for behavior on ATAPI devices due to unique considerations for posting a signature.

Tom Hanan stated that the proposal will be revised to include the text for modifying ATA/ATAPI-4.

7. Enhanced BIOS Disk Drive Technical Report - Project 1226DT

Curtis Stevens was not present. Rev 3 of the draft was available. The group repeated the request to switch to single column format to facilitate the use of pdf files. Changed note 1 in Table 2 to apply to the whole column.

Add a new paragraph for addressing capacity above 15,482,880 sectors (1024/240/63) (e.g. 7.9 GB) use the BIOS extensions in clause 3.

Table 2 describes the bit shift translation geometries that may be used to create altered geometries up to 15,482,880 sectors. Table 3 describes the bit shift translation that may be used to create altered geometries up to 16,455,560 sectors.

Add a bibliography of industry references for Int 13 definitions.

Lock levels greater than one need to be maintained by the BIOS.

The draft is technically complete but needs further editorial work. An editorial session is planned for the June meeting at 1600 on 6/17/97 assuming Curtis Stevens will be available.

7.1 Annex B changes from EDD

Curtis Stevens sent a message that what is in Annex B is aimed at hardware developers and should stay in D1153. The group agreed to Curtis's request.

8. Old Business**8.1 Items from Open Issues List****8.1.1 Synchronization of Status and Alternate Status with Busy**

See 9.2.

8.1.2 Should the "or" in Figure 13 be eliminated

Fixed in draft review.

8.1.3 Figure 17 - Should the requirement to release when the Bus Device Release Interrupt is enabled be removed?

Non-issue.

8.2 Support for Removable Media [Miller & Mayne] (D97120)

An issue of the lock count needs investigation. The proposal only provides support for one lock level in the device. There seemed to be agreement that lock levels greater than one are handled by the host and not the device.

Tom Hanan moved and Peter McLean seconded that word 127 be implemented as specified and bits 2-15 be reserved. The motion passed unanimously.

Conflict with Ultra definition of bits for DMA operations. To eliminate the conflict the sense of the group was to delete Read Protect from the proposal.

Add bit 4 to word 86 and 83 to report feature enabled. (This was bit 3 until late in the day when it came to our attention that APM was already assigned bit 3.)

A revision with these changes will be forthcoming.

Conflict with WRITE VERIFY error register. The sense of the group was to make WRITE VERIFY abort if MSN is enabled or make it obsolete. The group is instructed to investigate the ramifications of these actions.

8.3 Tailgate [McLean] (D97107)

Pete McLean reported that there were no new technical issues at the last meeting. An editorial review is scheduled for Tuesday, June 17, 1997. There is some indication that a proposal for technical change may be brought into this meeting.

8.4 PDIAG in 80 Conductor cable [Evans] (D97121)

Mark Evans reviewed the proposal.

Tom Hanan pointed out that some older devices ground this signal for a long enough period of time that it may be detected as an 80-conductor cable. Add recommendation to downshift if errors are detected and host should check the IDENTIFY DEVICE data for ATA-3 and/or Ultra DMA support.

8.5 44 & 66 MTS [Evans] (D97117r0)

Deferred.

8.6 Advanced Power Management [Colegrove] (D97126)

Dan Colegrove reported that the revision 1 contains the updates from the last meeting. Dan Colegrove moved and Totani-san seconded that APM be recommended for inclusion into ATA/ATAPI-4 with the table modified to include all values. The motion passed unanimously.

8.7 Cable Select [Goodfellow] (D97129)

See 8.4.

9. New Business**9.1 Making Execute Device Diagnostics Obsolete [] ()**

.There was strong objection to making to the suggestion.

9.2 PIO Response Tables for Annex E [Landis] (D97134r0)

Hale Landis described the purpose of D97134r0 and pointed out a few changes he was going to make to the proposed tables. The group suggested some other clarifications. Hale requested that the group review the proposal for further discussion at the June meeting.

9.3 T13 Reflector

Tom Hanan described the improvements that had been made in the reflector. The group thanked Tom for these enhancements. The new address of t13@dt.wdc.com has been activated but the old alias will continue to work for a while. The service provider for ftp in some portions of the country has been changed. The Colorado contingent noted that they had noticed a marked increase in performance.

10. Call for Patents

This is a regular agenda item to identify any potential patent issues with developing standards.

A document is available from ANSI, "Procedures for the Development and Coordination of American National Standards", at no charge. Annex I contains the ANSI patent policy.

The Chair requested that any participant aware of patents or patent disclosures that may be required to comply with any publications resulting from T13 projects provide an early disclosure of such patent and offer to license such patents under reasonable and non-discriminatory conditions in accordance with the ANSI Patent Policy.

11. Open Issues List Summary

The following items were added to the list at this meeting:

9) Some QIC devices are setting the CHECK bit when BSY=0. (Note: An Email subsequent to the meeting withdrew the assertion.)

10) Conflict with WP bit and UNC consider Make WRITE VERIFY obsolete to eliminate conflict with RMSN.

11) Location of DD7 pull down resistor with Ultra DMA.

12. Review of New Action Items

None.

13. Meeting Schedule

The next plenary meeting of T13 will be July 25, 1997 at the Seagate Technology facility, in San Jose, CA hosted by Seagate Technology.

The next working group meeting will be June 18-20, 1997 at the Western Digital facility, in Irvine, CA hosted by Western Digital. (With an EDD editorial session tentatively set for 1600 the day before.)

The subsequent working group meeting will be July 23-24, 1997 at the Seagate Technology facility, in San Jose, CA hosted by Seagate Technology.

The long term meeting schedule is:

Date	Location	Host	Contact
June 18-20, 1997	Irvine, CA	Western Digital	Tom Hanan
July 23-25, 1997 *	San Jose, CA	Seagate	Marc Noblitt
August 20-22, 1997	Longmont, CA	SSI/TI	Yogi Schaffner
September 24-26, 1997	Irvine, CA	Phoenix Technologies	Curtis Stevens
October 22-24, 1997*	Wailea, Maui, HI	Quantum	Mark Evans
December 3-5, 1997	Irvine, CA	Western Digital	Tom Hanan
January 21-23, 1998+			Marc Noblitt
February 17-20, 1998*	Ft. Collins	Symbios Logic	Dave Evans
March 25-27, 1998+			Marc Noblitt
April 14-17, 1998 *	Irvine, CA	Western Digital	Tom Hanan
May 20-22, 1998+			Marc Noblitt
June 16-19, 1998*	Irvine, CA	WD	Tom Hanan
July 22-24, 1998 +			Marc Noblitt
August 18-21, 1998*	Boulder	Maxtor	McLean
September 23-25, 1998+			Marc Noblitt
October 20-23, 1998*	Wailea, Maui, HI	Quantum	Mark Evans
December 1-4, 1998*	Irvine, CA	Western Digital	Tom Hanan

* indicates that Friday will be used for the plenary meeting.

+ indicates this meeting is tentative and may be canceled.

14. Adjournment

The meeting was adjourned upon completion of all the agenda items.