

X3T13/D96104r6

24 June 1996

ATA Overlap Proposal

Point of contact:

Pete McLean
Maxtor Corporation
2190 Miller Drive
Longmont, CO 80501-6744
USA

Tel: 303-678-2149
Fax: 303-682-4811
Email: pete_mclean@maxtor.com

Scope

This document presents the detailed text changes to the ATA-3 document (X3T10/2008Dr6) for the Overlap proposal. It is based on the Overlap proposal submitted by Western Digital Corporation (X3T10/95-258r0) with the changes presented by Quantum Corporation (X3T10/95-257r0).

The text to be added to Clause 7 is presented first to provide an introduction to overlap and command queuing. The remainder of the document presents material in the order that it will appear in the ATA document.

Revision History

Revision 1 - Draft created from WD proposal X3T10/95-258r1

Revision 2 - Protocol diagram added

Revision 3 - Added timing diagram. Made revisions requested at page by page review at 24 August 1995 meeting.

Revision 4 - Removed PIO commands, added state diagram and timing diagrams. Major editorial changes.

Revision D96104r1 - Added selected as a state bit in state and timing diagrams.

Revision D96104r2 - Replaced Proxy interrupt with proposal D96105r1. Made editorial changes requested by John Masiewicz.

Revision D96104r3 - Added configuration description in 7.*. Modified text as requested at March 27-29 meetings.

Revision D96104r4 - Made error register like PACKET command error register, added IDENTIFY DEVICE changes to IDENTIFY PACKET DEVICE, showed that PACKET command data transfers can be split but READ/WRITE DMA OVERLAP cannot, made text changes as requested.

Revision D96104r5 - Removed high assertion shared interrupt. Made text changes requested at May 22 meeting.

Revision D96104r6 - Removed UIRQ bit and PDIAG- handshake. Added INTP, Interrupt Pending bit.

7.* Command overlap and command queuing feature set

Command overlap is an optional feature that allows a host to issue commands or service outstanding commands with one device while a command is outstanding to the second device. For example, the host may issue a command to the first device and before the command is completed (i.e., requested data is transferred) , select the second device and issue the second device a command.

Command queuing is an optional feature that allows a host to have concurrent commands outstanding to a given device. That is, before a first command has completed (i.e., requested data is transferred) additional commands may be issued to the device. A device that supports command queuing shall also support command overlap.

A device that supports the command overlap feature set may be configured on the bus with a device that does not support command overlap. For this configuration, the Overlapped INTRQ feature shall not be enabled in the device that supports command overlap. The host may issue an overlapped command to the device supporting that command, then select the other device, and issue it a command. Since the second device does not support overlap, the host must keep that device selected until the command completes and BSY is set to zero. The host may then select the first device and transfer the data associated with the overlapped command. Figure xx shows an example of this operation. In this example, the overlap device shall not assert INTRQ unless selected so the host must reselect the overlap device after completing the command with the non overlap device to be interrupted when the overlap device is ready to transfer the data.

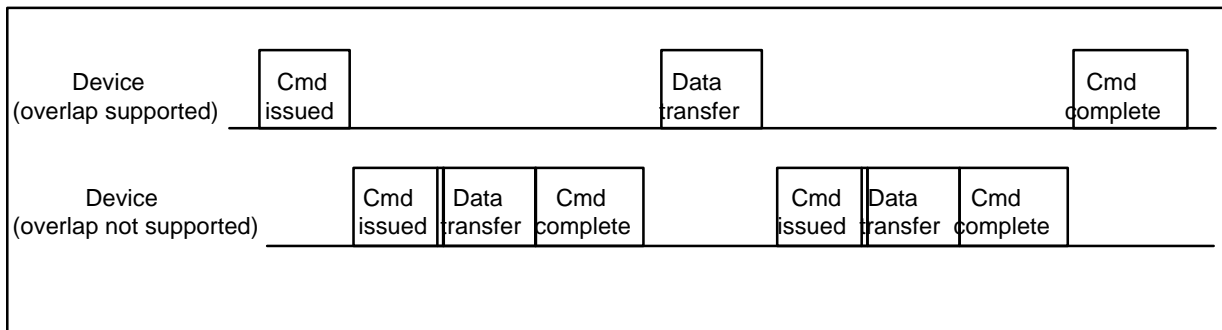


Figure xx - Example of command overlap with only one overlapping device

A device that supports the command overlap feature set may be configured on the bus with a device that does not support command overlap but supports the PACKET command feature set. For this configuration, the Overlapped INTRQ feature shall not be enabled in the device that supports command overlap. The host may issue an overlapped command to the device supporting that command, then select the other device, and issue it a command. If the Command is a PACKET command with overlap set, the host may then select the first device and transfer the data associated with the overlapped command. Having completed that command, the host may select the second device and complete its command. Notice that the data transfer of the PACKET command may be split but the data transfer of the READ/WRITE DMA OVERLAP commands may not. Figure yy shows an example of this operation. In this example, the devices shall not assert INTRQ unless selected so the host must reselect a device to be interrupted when the device is ready to transfer the data.

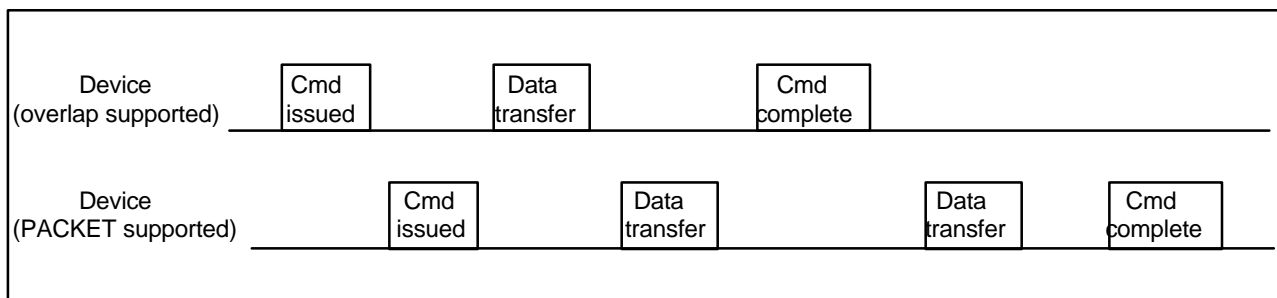


Figure yy - Example of overlap with PACKET feature set device

When two devices that support overlap are configured on a bus, Overlapped INTRQ shall be enabled. Overlapped commands may then be issued as shown in figure yy but the devices may interrupt the host when ready to transfer data regardless of device selection.

7.*.1 Command Overlap

Command overlap is accomplished by the use of the following mechanisms.

1. Information in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response that notifies the host that the device supports the command overlap feature.
2. The SET FEATURES command that allows the host to enable the command overlap feature.
3. An overlap command set that identifies those commands that may be overlapped.
4. A mechanism called Release that allows the host to select the second device when the first device has an overlapped command outstanding.
5. An Overlapped INTRQ implementation that allows an unselected device to interrupt. This mechanism shall only be enabled when both devices support command overlap.
6. A SERVICE command that allows the host to reselect a device that has an overlapped command outstanding so that command execution may be continued.

7.*.1.1 Overlap IDENTIFY DEVICE information

Bits in word 73 in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response informs the host if the device supports Command Overlap and Command Queuing. Word 71 informs the host of the maximum time from the issuing of an overlap command to the negation of BSY during the Release process. Word 72 informs the host of the maximum time from the issuing of a SERVICE command to the negation of BSY during the Release process. See Clause *.*; IDENTIFY DEVICE.

7.*.1.2 Overlap SET FEATURES command

The issuing of a SET FEATURES command with the Features register content 5Fh or DFh, enables or disables the use of the Overlapped Interrupt mechanism.

The issuing of a SET FEATURES command with the Features register content 5Dh or DDh, enables or disables the issuing of an interrupt when the Release process has completed (i.e., BSY negated) after the issuing of an overlapped command. This allows a host to poll the BSY bit or receive an interrupt.

The issuing of a SET FEATURES command with the Features register content 5Eh or DEh, enables or disables the issuing of an interrupt when BSY is cleared to zero after the issuing of a SERVICE command. This allows a host to poll the BSY bit or receive an interrupt when the BSY bit is negated.

See Clause **, SET FEATURES.

7.*.1.3 Overlap commands

The only commands that shall be overlapped are PACKET, READ DMA OVERLAP, and WRITE DMA OVERLAP.

Upon the receipt of an overlapped command, the device shall “save” the command and its required parameters.

The host shall only issue the SERVICE command when an overlapped command is outstanding to the device requiring service and the device has released. The contents of the Features, Sector Count, Alternate Status, and Status registers are redefined for the issuing of these commands and remain redefined until the completion of these commands. See **, **, and **.

For the READ DMA OVERLAP and WRITE DMA OVERLAP commands all requested data shall be transferred in a single operation, that is, the data transfer shall not be split by releasing the bus during the transfer. The PACKET command allows the data transfer to be split by releasing the bus after only a portion of the data has been transferred, then requesting service and continuing the transfer after a SERVICE command.

If an overlap command is issued while a non overlap command is in progress, both the command in progress and the newly issued command shall be aborted. The ending status shall be aborted command and the results are indeterminant.

7.*.1.4 Release

Upon the receipt of an overlapped command, the device shall “save” the command and its required parameters.

If the release interrupt has been enabled via the SET FEATURES command, the device shall release the bus and no data shall be transferred. The device shall release by setting REL , clearing BSY and asserting INTRQ regardless of whether the data is ready to transfer or not.

If the release interrupt has not been enabled via the SET FEATURES command, the device may either release or transfer data immediately if the data is available. To release, the device sets REL and clears BSY, freeing the bus for the selection of the other device. To transfer the data immediately, the device sets DRQ and DMARQ, clears BSY and waits for the host to transfer the data.

Once the REL bit has been set indicating that the device has released an overlap command in progress, the REL bit shall remain set until a new command is received.

The typical time from the receipt of an overlap command to the negation of BSY for a release is reported in Word 72 of the IDENTIFY DEVICE response.

Once the Release process has completed, the host may select the other device if it desires.

7.*.1.5 Overlapped interrupt

The overlapped interrupt mechanism allows an unselected device to interrupt the host. The feature is enabled via the 5Fh SET FEATURES command and shall be enabled for overlapped operation in both devices if both devices support it. When enabled, the overlapped interrupt mechanism shall be used for interrupts associated with all commands regardless whether the command may be overlapped or not. For overlapped interrupts, INTRQ shall be a low asserted, wire-or signal.

When the overlapped interrupt is used, the host shall monitor the state of INTRQ rather than looking for a transition. This is required since when two devices are asserting INTRQ and the Status register of one is read, INTRQ is still asserted by the second device. The host has to be aware that there may be a second device interrupting and service that interrupt after servicing the interrupt of the first device.

When overlapped interrupt is enabled, a device shall set INTP, Interrupt Pending, bit 1 of the Status register to one, when the device has a pending interrupt.

7.*.1.6 SERVICE command

The SERVICE command is issued by the host to reselect a device that has an overlapped command outstanding and has released. The SERVICE command shall only be issued when the device has an overlapped command outstanding and has released. When a device that has released overlap command outstanding is ready to transfer data, the device sets the SERVICE bit and asserts INTRQ if Overlapped INTRQ is enabled or if selected.

Upon receipt of the SERVICE command, the device shall assert BSY, set the command tag and interrupt reason in the Sector Count register, clear SERVICE, set DRQ and DMARQ, then negate BSY. If the 5Eh SET FEATURES command is enabled, the device shall assert INTRQ after BSY has been negated. This allows the host to check the status associated with the overlapped command and continue the execution of the command.

7.*.2 Command queuing

Command queuing allows the host to issue concurrent commands to the same device. Only overlapped commands may be queued. If a queued command is outstanding when a non-queued command is received both commands and the queue will be aborted. The ending status shall be ABORT command and the results are indeterminant.

The maximum queue depth supported by a device shall be indicated in word 73 of the IDENTIFY DEVICE response.

A queued command shall have a tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this tag shall be restored so that the host can identify the command for which status is being presented. If a queued command is issued with a tag value that is identical to the tag value for a command already in the queue, the entire queue shall be aborted including the new command. The ending status shall be ABORT command and the results are indeterminant. If an error causes the queue to be aborted, the QA bit shall be set in the register.

3.1 Definitions and abbreviations~~(add)~~

Command overlap - Command overlap is an optional feature that allows a host to issue commands or service outstanding commands with one device while a command is outstanding to the second device.

Command queuing - Command queuing is an optional feature that allows a host to have concurrent commands outstanding to a given device.

Overlapped interrupt - The Overlapped Interrupt mechanism that allows an unselected device to signal the host that it wishes to continue execution of an outstanding overlapped command.

Release - A mechanism that allows the host to select the second device when the first device has an overlapped command outstanding.

5.2.10 INTRQ (Device interrupt)(add)

When both devices attached to the interface are capable of overlapped operation and they are enabled for Overlapped interrupts. The Overlapped interrupt feature is enabled via the 5Fh SET FEATURES command. When overlapped interrupt is enabled, the INTRQ is a low asserted, wire-or signal.

|

8.7 IDENTIFY DEVICE(add)

Table 14 - Identify Device Information (add)

Word	F/V	
73		Capabilities
	F	15 Interleaved DMA supported
	F	14 Command queuing supported
	F	13 Overlap operation supported
	F	12 Overlapped interrupt supported
	F	4-0 Maximum queue depth the device supports
71	F	Typical time for Release after overlap command receipt in μ sec
72	F	Typical time for Release after SERVICE command receipt in μ sec

8.7.* Interleaved DMA support

Bit 15 of word 73 is used to indicated that the device supports interleaved DMA data transfer for overlapped DMA commands.

8.7.* Command Queuing supported

Bit 14 of word 73 is used to indicated that the device supports command queuing for overlapped commands.

8.7.* Command overlap supported

Bit 13 of word 73 is used to indicated that the device supports command overlap operation.

8.7.* Overlapped interrupt supported

Bit 12 of word 73 is used to indicate that the device supports overlapped interrupts.

8.7.* Maximum queue depth supported

Bits 4 through 0 of word 73 indicate the maximum queue depth supported by the device. If bit 14 of word 73 is zero indicating that the device does not support command queuing, the value in this field shall be 00h.

8.7.* Time for release after overlap command receipt

If bit 13 in word 73 is set indicating the device supports command overlap, the value in word 71 shall be the typical time for release after an overlap command receipt in μ sec. If bit 13 in word 73 is cleared indicating the device does not support command overlap, the value in word 71 shall be 00h.

8.7.* Time for release after SERVICE command receipt

If bit 13 in word 73 is set indicating the device supports command overlap, the value in word 72 shall be the typical time for release after an overlap command receipt in μ sec. If bit 13 in word 73 is cleared indicating the device does not support command overlap, the value in word 72 shall be 00h.

8.9 IDENTIFY PACKET DEVICE^(add)

Table 14 - Identify Device Information (add)

Word	F/V	
73		Capabilities
	F	15 Interleaved DMA supported
	F	14 Command queuing supported
	F	13 Overlap operation supported
	F	12 Overlapped interrupt supported
	F	4-0 Maximum queue depth the device supports
71	F	Typical time for Release after overlap command receipt in μ sec
72	F	Typical time for Release after SERVICE command receipt in μ sec

8.7.* Interleaved DMA support

Bit 15 of word 73 is used to indicated that the device supports interleaved DMA data transfer for overlapped DMA commands.

8.7.* Command Queuing supported

Bit 14 of word 73 is used to indicated that the device supports command queuing for overlapped commands.

8.7.* Command overlap supported

Bit 13 of word 73 is used to indicated that the device supports command overlap operation.

8.7.*Overlapped interrupt supported

Bit 12 of word 73 is used to indicate that the device supports overlapped interrupts.

8.7.* Maximum queue depth supported

Bits 4 through 0 of word 73 indicate the maximum queue depth supported by the device. If bit 14 of word 73 is zero indicating that the device does not support command queuing, the value in this field shall be 00h.

8.7.* Time for release after overlap command receipt

If bit 13 in word 73 is set indicating the device supports command overlap, the value in word 71 shall be the typical time for release after an overlap command receipt in μ sec. If bit 13 in word 73 is cleared indicating the device does not support command overlap, the value in word 71 shall be 00h.

8.7.* Time for release after SERVICE command receipt

If bit 13 in word 73 is set indicating the device supports command overlap, the value in word 72 shall be the typical time for release after an overlap command receipt in μ sec. If bit 13 in word 73 is cleared indicating the device does not support command overlap, the value in word 72 shall be 00h.

8.* READ DMA OVERLAP

OPCODE - C7h

TYPE - Optional

PROTOCOL - DMA data in overlap

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the starting sector address to be read and whether the address is CHS or LBA. The Features register specifies the number of sectors to be transferred. The Sector Count register contains the tag for this command if the device supports command queuing.

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C7h							

NORMAL OUTPUTS -

If the device has the requested data ready to transfer when the command is received, the device may transfer the data without releasing the bus. The register contents shall be set as shown below to execute the transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be cleared to zero.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero.

Bit 3 - DRQ - This bit shall be set to one.

Bit 2 - CORR - As described in .

Bit 1 - **INTP** - This bit shall be set to one indicating the device has an interrupt pending. .

Bit 0 - ERR - This bit shall be cleared to zero.

If the device releases during the execution of this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag				REL	na	na	
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY		SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be set indicating that the device has released an overlap command.

Bits 1-0 This field shall be zeros.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.

Bit 3 - DRQ - This bit shall be cleared to zero.

Bit 2 - CORR - This bit shall be cleared to zero.

Bit 1 - INTP - This bit shall be set to one indicating the device has an interrupt pending .

Bit 0 - ERR - This bit shall be cleared to zero.

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag				REL	na	na	
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be cleared to zero.

Bits 1-0 This field shall be zeros.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero.

Bit 3 - DRQ - This bit shall be cleared to zero.

Bit 2 - CORR - As described in .

Bit 1 - **INTP** - This bit shall be set to one indicating the device has an interrupt pending.

Bit 0 - **ERR** - This bit shall be cleared to zero.

ERROR OUTPUTS - The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort and the QA bit to be set. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	Error code				MCR	ABRT	na	AMNF
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Bits 7-4 Error code

00h - no error

03h - Uncorrectable error has been detected

06h - Indicates new media is available to the host

09h - Indicates the device has aborted its queue

0Ah - Indicates the device could not find the requested sector ID field

Bit 3 - Indicates that a request for media removal has been detected by the device

Bit 2 - Indicates this command is not supported

Bit 0 - Indicates that the data address mark has not been found after finding the correct ID field

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to a READ DMA command. If the release interrupt has been enabled via a SET FEATURES command, the device shall release the bus when the command and its parameters have been "saved". If the release interrupt has been disabled via the SET FEATURES command, the device may release the bus or it may execute the data transfer without release if the data is ready to transfer.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

8.* SERVICE

OPCODE - A2h

TYPE - Optional

PROTOCOL - Non-data command

INPUTS -

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Command	A2h							

NORMAL OUTPUTS -

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	IO	C/D-
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be set to one.

Bit 1 - IO - This bit shall be cleared to zero indicating that the data transfer is from host to device if the command being serviced is a write command. This bit shall be set to one indicating that the data transfer is from device to host if the command being serviced is a read command.

Bit 0 - C/D- - This bit shall be cleared to zero indicating that data is to be transferred.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero.

Bit 3 - DRQ - This bit shall be set to one.

Bit 2 - CORR - As described in .

Bit 1 - **INTP** - This bit shall be set to one indicating the device has an interrupt pending .

Bit 0 - ERR - This bit shall be cleared to zero.

ERROR OUTPUTS - Aborted command if the device does not support this command. Aborted error if no overlap command is currently in progress.

Status register				Error register					
DRDY	DF	CORR	ERR	QA	BBK	UNC	IDNF	ARBT	AMNF
V	V	na	V	na	na	na	na	V	na

PREREQUISITES - This command shall be issued only when there is an overlap command in progress.

DESCRIPTION - Upon receipt of this command, the device shall set BSY, place the parameters for the command requiring service in the appropriate registers, and then clear BSY.

8.28 SET FEATURES^(add)

Table 19 - Set Features register definitions (add)

Value	
5Dh	Enable interrupt for Release after the receipt of an overlap command.
5Eh	Enable interrupt after the processing of a SERVICE command.
5Fh	Enable Overlapped interrupt
DDh	Disable interrupt for Release after the receipt of an overlap command.
DEh	Disable interrupt after the processing of a SERVICE command.
DFh	Disable Overlapped interrupt

8.28.* Enable/disable release interrupt

Subcommand codes 5Dh and DDh allow a host to enable or disable the assertion of an interrupt when a device executing an overlap command releases the bus.

8.28.* Enable/disable SERVICE interrupt

Subcommand codes 5Eh and DEh allow a host to enable or disable the assertion of an interrupt when the device is ready to transfer at the completion of a SERVICE command.

8.28.* Enable/disable Overlapped interrupts

Subcommand codes 5Fh and DFh allow a host to enable the use of overlapped interrupts or to disable this feature. Overlapped interrupts shall only be enabled when both devices are capable of overlapped interrupts. Since a configuration with one device using overlapped interrupts and the second device not using overlapped interrupts causes electrical conflict, the following algorithm shall be used when enabling overlapped interrupts.

1. The host shall insure that neither device has a command in progress.
2. The host shall select a device and enable overlapped interrupts.
3. The device shall interrupt upon completion of this command as though overlapped interrupts were not enabled.
4. The host shall select the other device and enable overlapped interrupts.
5. The device shall interrupt upon completion of this command as though overlapped interrupts were not enabled.
6. Devices shall respond to all subsequent commands with overlapped interrupts.

The following algorithm shall be used when disabling overlapped interrupts.

1. The host shall insure that neither device has a command in progress.
2. The host shall select a device and disable overlapped interrupts.
3. The device shall interrupt upon completion of this command as though overlapped interrupts were enabled.
4. The host shall select the other device and disable overlapped interrupts.
5. The device shall interrupt upon completion of this command as though overlapped interrupts were enabled.
6. Devices shall respond to all subsequent commands with overlapped interrupts disabled.

8.* WRITE DMA OVERLAP

OPCODE - CCh

TYPE - Optional

PROTOCOL - DMA data out overlap

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the starting sector address to be written and whether the address is CHS or LBA. The Features register specifies the number of sectors to be transferred. The Sector Count register contains the tag for this command if the device supports command queuing.

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	CCh							

NORMAL OUTPUTS -

If the device is ready to accept the data when the command is received, the device may transfer the data without releasing the bus. The register contents shall be set as shown below to execute the transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be cleared to zero.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero.

Bit 3 - DRQ - This bit shall be set to one.

Bit 2 - CORR - As described in .

Bit 1 - **INTP** - This bit shall be set to one indicating the device has an interrupt pending.

Bit 0 - ERR - This bit shall be cleared to zero.

If the device releases during the execution of this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag				REL	na	na	
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be set indicating that the device has released an overlap command.

Bits 1-0 This field shall be zeros.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.

Bit 3 - DRQ - This bit shall be cleared to zero.

Bit 2 - CORR - This bit shall be cleared to zero.

Bit 1 - INTP - This bit shall be set to one indicating the device has an interrupt pending .

Bit 0 - ERR - This bit shall be cleared to zero.

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag				REL	na	na	
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL - This bit shall be cleared to zero.

Bits 1-0 This field shall be zeros.

Status register -

Bit 7 - BSY - This bit shall be cleared to zero.

Bit 6 - DRDY - As described in .

Bit 4 - SERV - This bit shall be cleared to zero.

Bit 3 - DRQ - This bit shall be cleared to zero.

Bit 2 - CORR - As described in .

Bit 1 - This bit shall be set to one indicating the device has an interrupt pending .

Bit 0 - ERR - This bit shall be cleared to zero.

ERROR OUTPUTS - The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort and the QA bit to be set. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	Error code				MCR	ABRT	na	AMNF
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	COR R	INTP	ERR

Bits 7-4 Error code

00h - no error

03h - Uncorrectable error has been detected

06h - Indicates new media is available to the host

09h - Indicates the device has aborted its queue

0Ah - Indicates the device could not find the requested sector ID field

Bit 3 - Indicates that a request for media removal has been detected by the device

Bit 2 - Indicates this command is not supported

Bit 0 - Indicates that the data address mark has not been found after finding the correct ID field

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to a Write DMA command. If the release interrupt has been enabled via a SET FEATURES command, the device shall release the bus when the command and its parameters have been "saved". If the release interrupt has been disabled via the SET FEATURES command, the device may release the bus or it may execute the data transfer without release if the device can accept the data.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

9.* Overlap command protocol

This class includes:

- READ DMA OVERLAP
- SERVICE
- WRITE DMA OVERLAP

Figure aa is a state diagram for the protocol for command overlap and command queuing commands. Figure BB provides an example of commands overlapped to two devices. Figure cc provides an example of two commands queued to a single device.

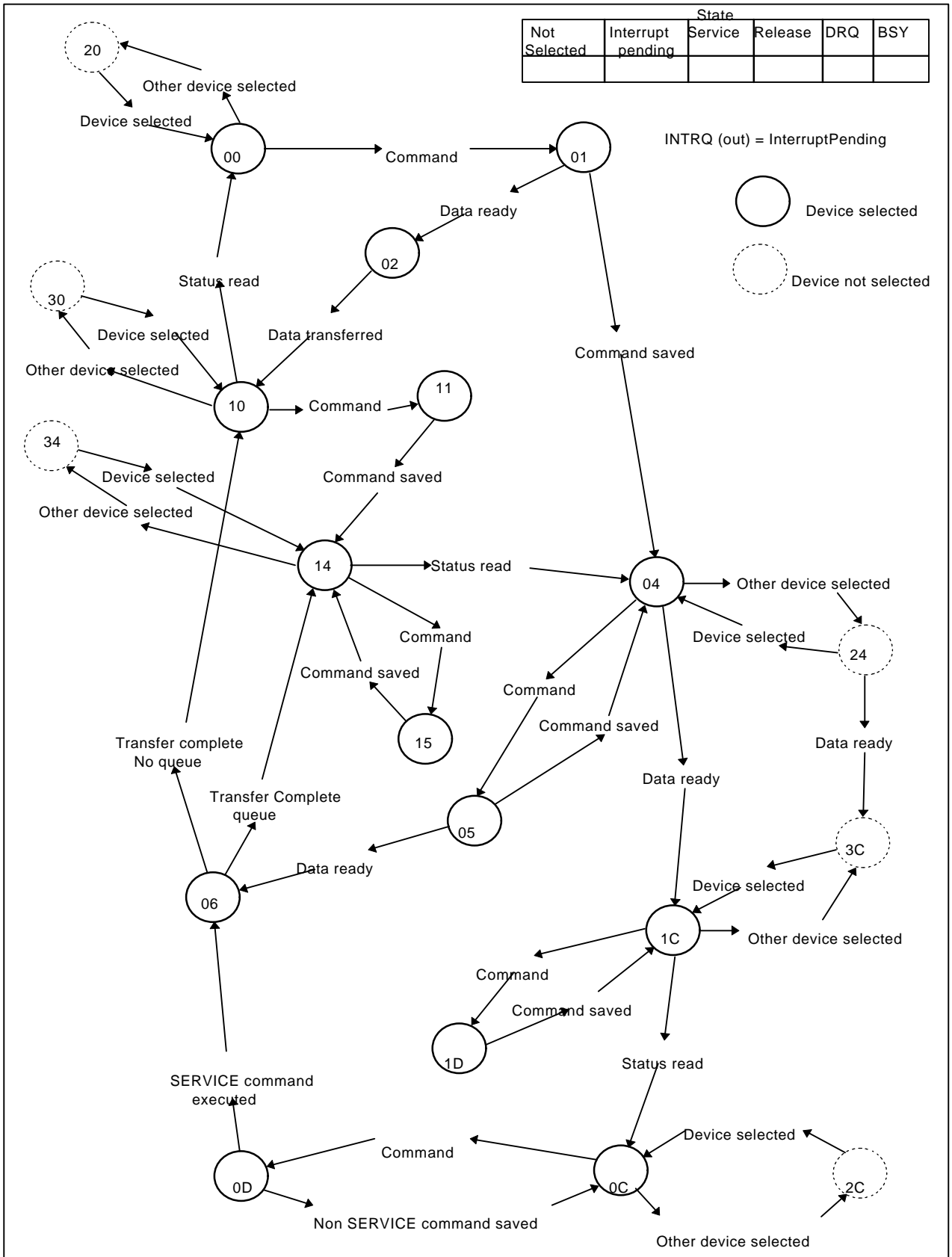


Figure aa - Command overlap and queuing state

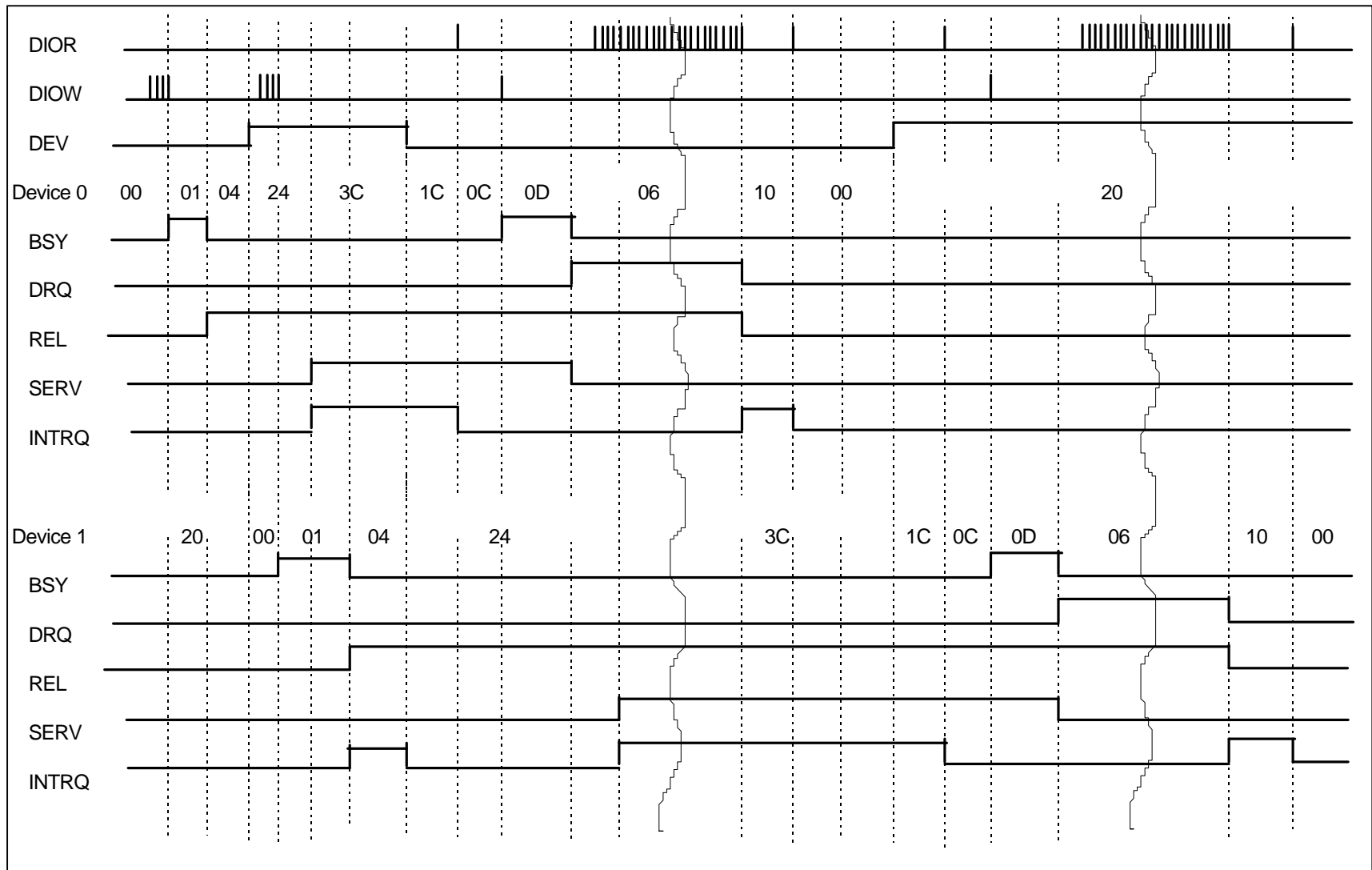


Figure bb - Two devices each with an overlapped command

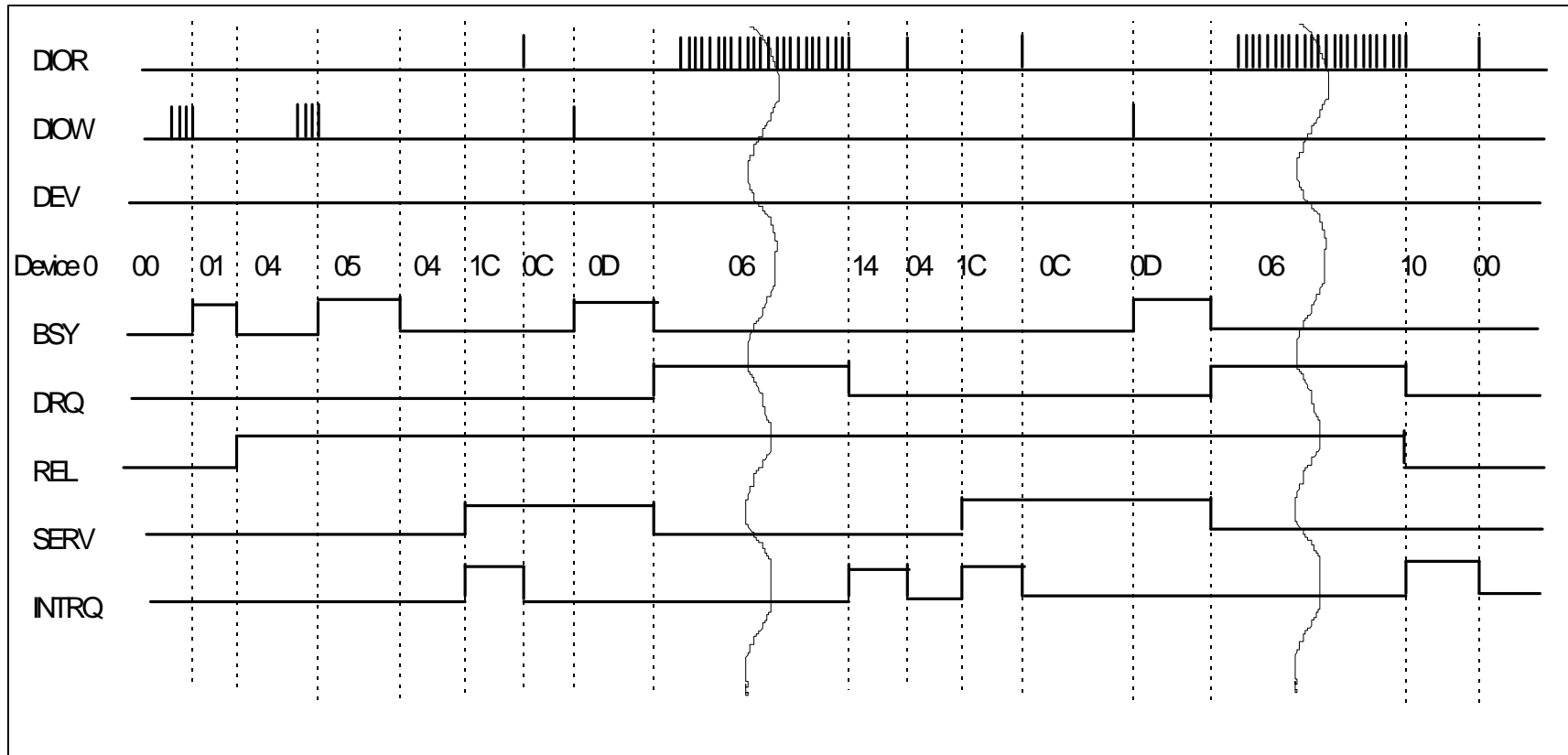


Figure cc - One device with two commands queued

Annex *

*****Editors Note: Should we create a new annex that includes Devon's diagrams for host behavior in overlap operation? *****