

X3T13/D96104r9

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ATA Overlap Proposal

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Scope

This document presents the detailed text changes to the ATA-3 document (X3T10/2008Dr6) for the Overlap proposal. It is based on the Overlap proposal submitted by Western Digital Corporation (X3T10/95-258r0) with the changes presented by Quantum Corporation (X3T10/95-257r0).

The text to be added to Clause 7 is presented first to provide an introduction to overlap and command queuing. The remainder of the document presents material in the order that it will appear in the ATA document.

Revision History

Revision 1 - Draft created from WD proposal X3T10/95-258r1

Revision 2 - Protocol diagram added

Revision 3 - Added timing diagram. Made revisions requested at page by page review at 24 August 1995 meeting.

Revision 4 - Removed PIO commands, added state diagram and timing diagrams. Major editorial changes.

Revision D96104r1 - Added selected as a state bit in state and timing diagrams.

Revision D96104r2 - Replaced Proxy interrupt with proposal D96105r1. Made editorial changes requested by John Masiewicz.

Revision D96104r3 - Added configuration description in 7.*. Modified text as requested at March 27-29 meetings.

Revision D96104r4 - Made error register like PACKET command error register, added IDENTIFY DEVICE changes to IDENTIFY PACKET DEVICE, showed that PACKET command data transfers can be split but READ/WRITE DMA OVERLAP cannot, made text changes as requested.

Revision D96104r5 - Removed high assertion shared interrupt. Made text changes requested at May 22 meeting.

Revision D96104r6 - Removed UIRQ bit and PDIAG- handshake. Added INTP, Interrupt Pending bit.

Revision D96104r7 - Removed shared INTRQ.

Revision D96104r8 - Removed INTP, state diagram, and timing diagrams. Added flow charts.

Revision D96104r9 - Removed PACKET command description added into D1153r7. Reduced document to just material required to add Read/write DMA overlapped/queued.

Replace 5.3.4 Overlapped PACKET commands with:

5.4 Overlapped commands

PACKET, READ DMA O/Q, and WRITE DMA O/Q commands may be overlapped. Overlap allows devices that require extended time to prepare for command execution to release the bus so that the other device on the bus may be used while the overlap device is preparing for the command execution. The act of releasing the bus involves clearing both the DRQ and BSY bits to zero just as at the end of a non-overlapped command.

For the PACKET command, overlap is indicated by the OVL bit in the features register when the PACKET command is issued.

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been enabled via the SET FEATURES command, the device must release when the command packet has been received. This allows the host to select the other device to execute commands if desired. When the device is ready to continue the command, the device sets SERV to one, and asserts INTRQ if selected and interrupts are enabled. The host then issues the SERVICE command to continue the execution of the command

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, the device may or may not release. If the device is to complete execution of the command, it may complete the command immediately as described in the non-overlap case. If the device is not ready to complete execution of the command, the device may release and complete the command as described in the previous paragraph.

For the READ DMA O/Q and WRITE DMA O/Q commands, the device may or may not release. If the device is to complete execution of the command, it may complete the command immediately. If the device is not ready to complete execution of the command, the device may release and complete the command via a service request.

Replace 5.3.5 Queued PACKET commands with:

5.5 Queued commands

Command queuing allows the host to issue concurrent commands to the same device. Only overlapped commands may be queued. If a queued command is outstanding when a non-queued command is received both commands and the queue will be aborted. The ending status shall be ABORT command and the results are indeterminant.

The maximum queue depth supported by a device shall be indicated in word 73 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

A queued command shall have a tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this tag shall be restored so that the host can identify the command for which status is being presented. If a queued command is issued with a tag value that is identical to the tag value for a command already in the queue, the entire queue shall be aborted including the new command. The ending status shall be ABORT command and the results are indeterminant. If an error causes the queue to be aborted, the QA bit shall be set in the register.

7.8 IDENTIFY DEVICE (add)

Table 8 - Identify Device Information (add)

Word	F/V		
73		Capabilities	
	F	15	reserved
	F	14	Command queuing supported
	F	13	Overlap operation supported
	F	12-5	reserved
F	4-0	Maximum queue depth the device supports	
83	F	1	1=READ/WRITE DMA O/Q supported
86	F	1	1=READ/WRITE DMA O/Q supported

7.8.* Command Queuing supported

Bit 14 of word 73 is used to indicated that the device supports command queuing for overlapped commands.

7.8.* Command overlap supported

Bit 13 of word 73 is used to indicated that the device supports command overlap operation.

7.8.* Maximum queue depth supported

Bits 4 through 0 of word 73 indicate the maximum queue depth supported by the device. If bit 14 of word 73 is zero indicating that the device does not support command queuing, the value in this field shall be 00h.

7.8.* Words 82-84: Features/command sets supported

If bit 1 of word 83 is set to one, the READ DMA O/Q and WRITE DMA O/Q commands are supported.

7.8.* Words 85-87: Features/command sets enabled

If bit 1 of word 86 is set to one, the READ DMA O/Q and WRITE DMA O/Q commands are supported.

7.* READ DMA O/Q

OPCODE - C7h

TYPE - Optional. Shall not be used by devices implementing the PACKET command feature set.

PROTOCOL - DMA O/Q.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C7h							

Features - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector count - if the device supports command queuing, bits (7:3) contain the tag for the command being delivered.

Sector number - starting sector number or LBA address bits (7:0).

Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address; bits (3:0) starting head number or LBA address bits (27:24).

NORMAL OUTPUTS -

If the device releases before transferring data for this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRD Y		SERV	DRQ	COR R	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL bit shall be set indicating that the device has released an overlap command.

Bits 1-0 shall be zeros.

Status register -

Bit 7 - BSY shall be cleared to zero.

Bit 6 - DRDY shall be set to one.

Bit 4 - SERV shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.

Bit 3 - DRQ bit shall be cleared to zero.

Bit 2 - CORR bit shall be cleared to zero.

Bit 0 - ERR bit shall be cleared to zero.

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	CORR	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL shall be cleared to zero.

Bits 1-0 shall be zeros.

Status register -

Bit 7 - BSY shall be cleared to zero.

Bit 6 - DRDY shall be set to one..

Bit 4 - SERV shall be cleared to zero.

Bit 3 - DRQ bit shall be cleared to zero.

Bit 2 - CORR shall be set to one if a correctable data error was found.

Bit 0 - ERR bit shall be cleared to zero.

ERROR OUTPUTS - The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort and the QA bit to be set. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	QA	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	Tag					REL	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	D	Head number or LBA			
Status	BSY	DRDY	na	SERV	DRQ	CORR	na	ERR

Error register -

- QA if error caused queue to be aborted.
- UNC if data is uncorrectable.
- IDNF if sector's ID field could not be found.
- ABRT if this command not supported>
- AMNF if the data address mark could not be found after finding the correct ID field.

Sector Number, Cylinder Low, Cylinder High, Device/Head - address of first unrecoverable error.

Status register -

- BSY shall be cleared to zero.
- DRDY shall be set to one.
- DF shall be set to one if a drive fault has occurred.
- DRQ shall be cleared to zero.
- CORR shall be set to one if a correctable data error was found.
- ERR shall be set to one if an Error register bit is set to one.

PREREQUISITES - DRDY set to one. The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to a READ DMA command. The device may release the bus or it may execute the data transfer without release if the data is ready to transfer.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

7.* Write DMA O/Q

OPCODE - CCh

TYPE - Optional. Shall not be used by devices implementing the PACKET command feature set.

PROTOCOL - DMA O/Q.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C7h							

Features - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector count - if the device supports command queuing, bits (7:3) contain the tag for the command being delivered.

Sector number - starting sector number or LBA address bits (7:0).

Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8).

Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16).

Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address; bits (3:0) starting head number or LBA address bits (27:24).

NORMAL OUTPUTS -

If the device releases before transferring data for this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRD Y		SERV	DRQ	na	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL bit shall be set indicating that the device has released an overlap command.

Bits 1-0 shall be zeros.

Status register -

Bit 7 - BSY shall be cleared to zero.

Bit 6 - DRDY shall be set to one.

Bit 4 - SERV shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.

Bit 3 - DRQ bit shall be cleared to zero.

Bit 0 - ERR bit shall be cleared to zero.

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	na	na
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRD Y	na	SERV	DRQ	na	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.

Bit 2 - REL shall be cleared to zero.

Bits 1-0 shall be zeros.

Status register -

Bit 7 - BSY shall be cleared to zero.

Bit 6 - DRDY shall be set to one..

Bit 4 - SERV shall be cleared to zero.

Bit 3 - DRQ bit shall be cleared to zero.

Bit 0 - ERR bit shall be cleared to zero.

ERROR OUTPUTS - The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort and the QA bit to be set. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	QA	na	na	IDNF	na	ABRT	na	na
Sector Count	Tag					REL	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	D	Head number or LBA			
Status	BSY	DRD Y	DF	SERV	DRQ	na	na	ERR

Error register -

QA if error caused queue to be aborted

IDNF if sector's ID field could not be found.

ABRT if this command not supported.

Sector Number, Cylinder Low, Cylinder High, Device/Head - address of first unrecoverable error.
Status register -

BSY shall be cleared to zero.

DRDY shall be set to one.

DF shall be set to one if a drive fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

PREREQUISITES - DRDY set to one. The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to a WRITE DMA command. The device may release the bus or it may execute the data transfer without release if the data is ready to transfer.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

8.* READ/WRITE DMA O/Q command protocol

This class includes:

- READ DMA O/Q
- SERVICE
- WRITE DMA O/Q

Figure nn describes the execution of a READ DMA O/Q or WRITE DMA O/Q command.

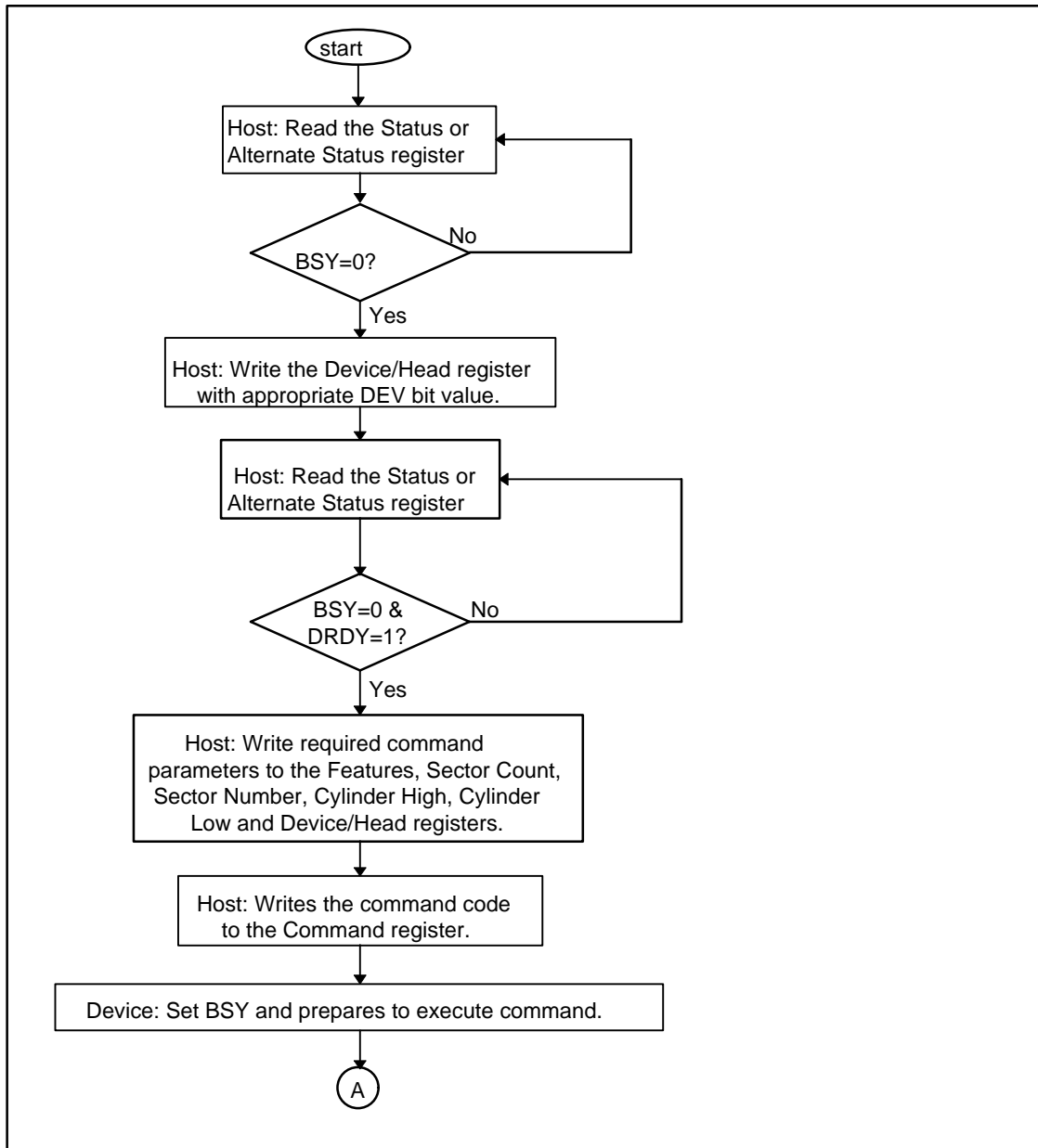


Figure nn – READ/WRITE DMA O/Q command (continued)

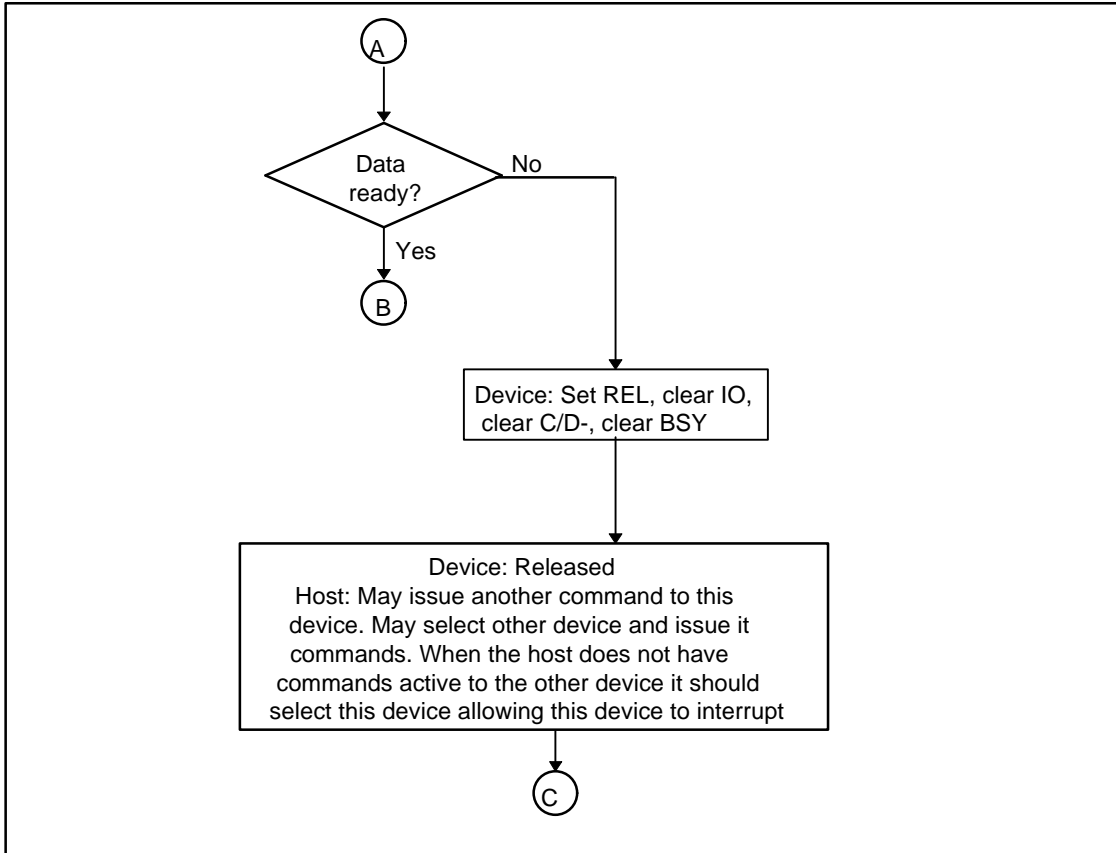


Figure nn – READ/WRITE DMA O/Q command(continued)

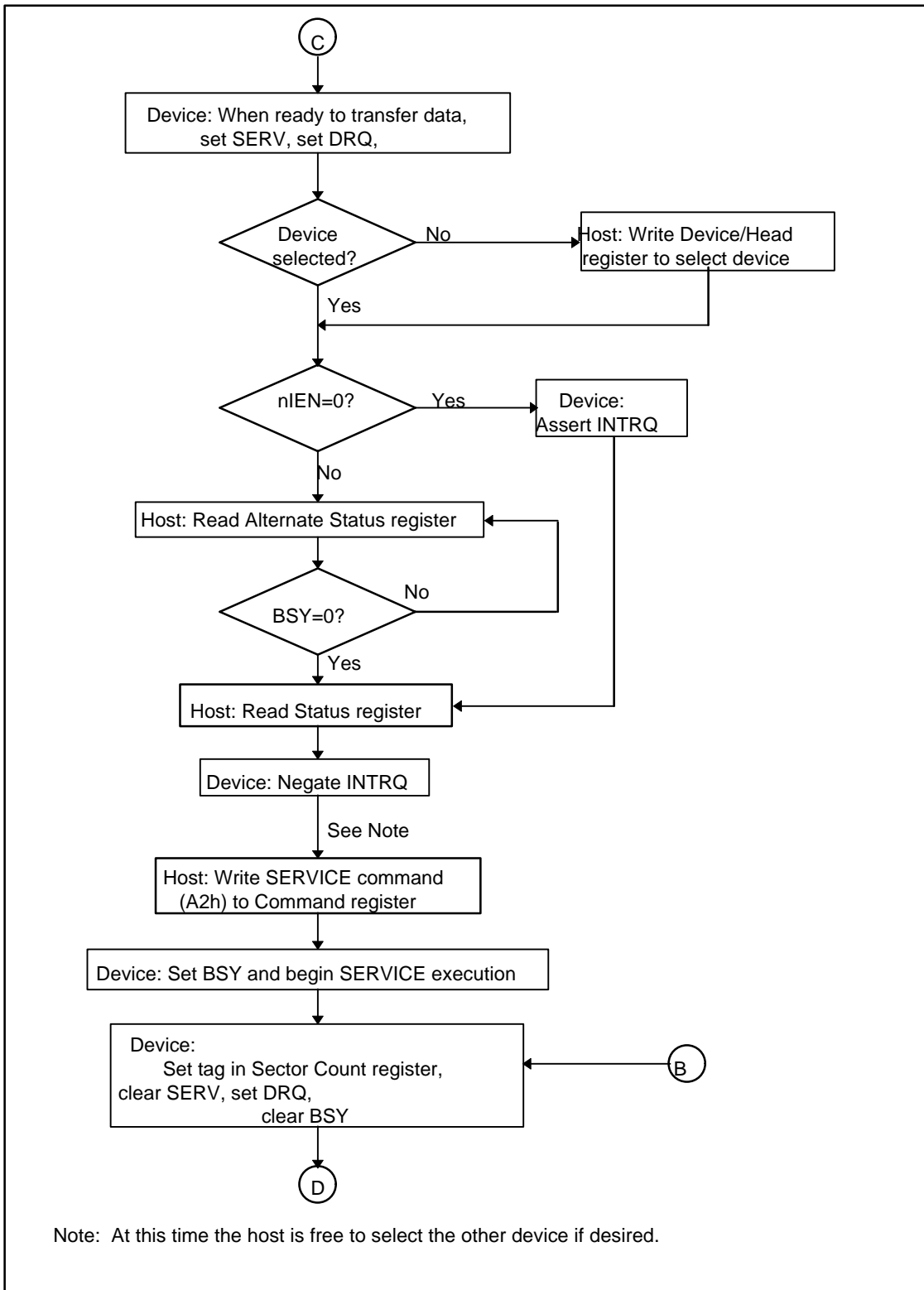


Figure nn – READ/WRITE DMA O/Q command(continued)

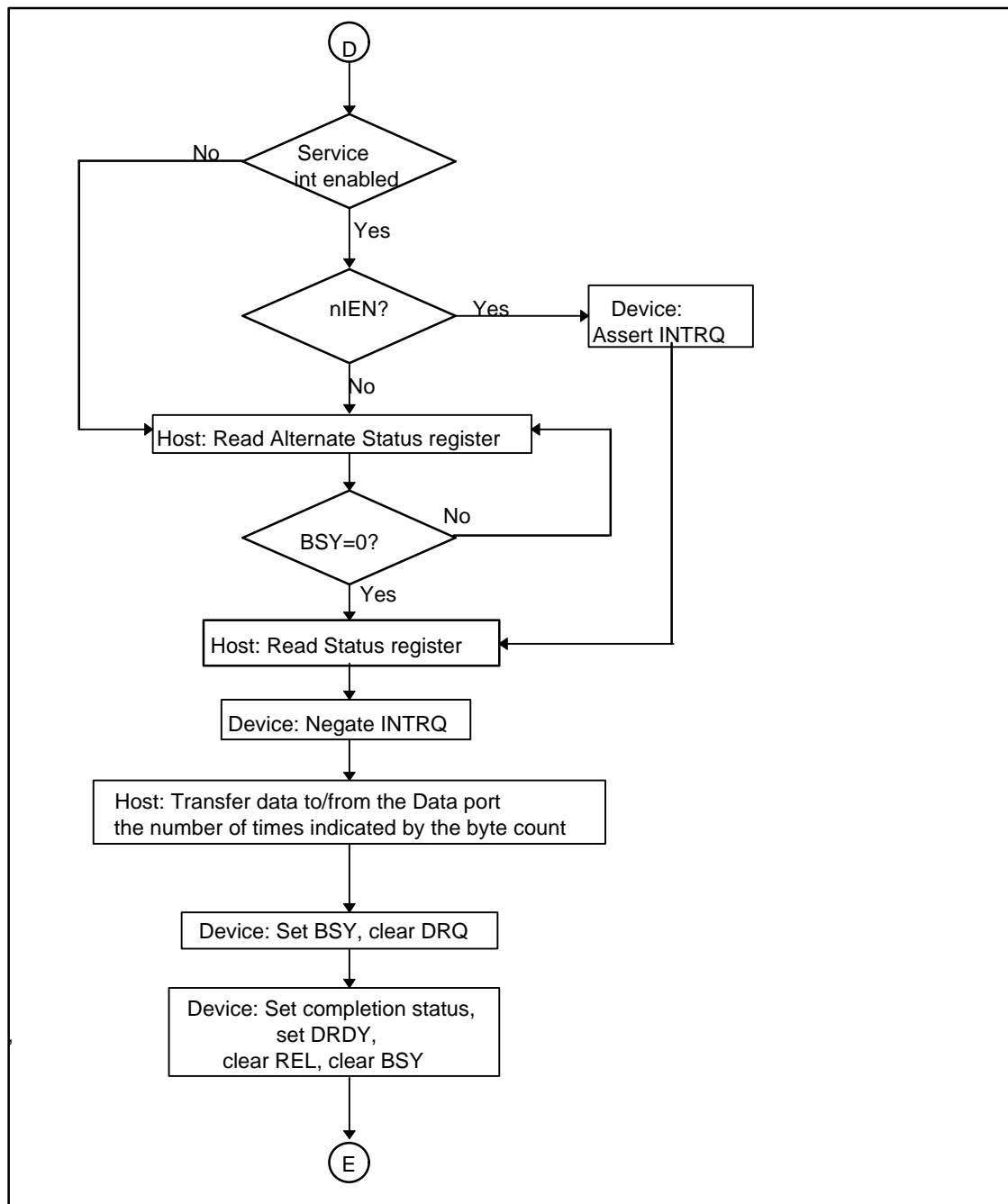


Figure nn – READ/WRITE DMA O/Q command(continued)

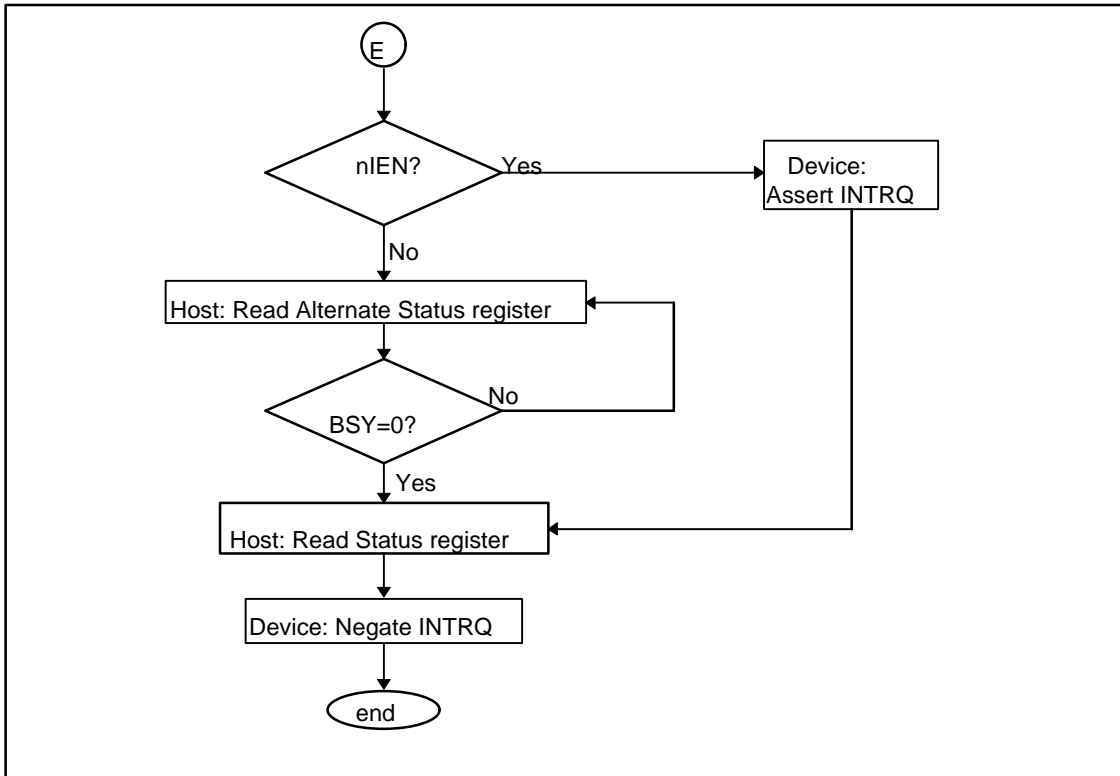


Figure nn – READ/WRITE DMA O/Q command(*concluded*)