

## Proposal for removing redundant information in ATA/ATAPI-4

Pete McLean  
 Maxtor Corp.  
 2190 Miller Drive  
 Longmont, CO 80501  
 303 678-2149  
 pete\_mclean@maxtor.com  
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**Purpose:** In many cases, the same items are specified in numerous locations throughout the document. In some cases, what is specified is in fact different in different locations. This proposal is intended to insure that each item is specified in only one location and that this location is the logical location for the specified material.

### Overview:

#### 1. Driver and termination definition

The logical signal definitions for DASP, IORDY, PDIAG, and CSEL in clause 5 contain descriptions of drivers and/or termination. The remaining signal definitions do not. Table 4 in clause 4 contains this information for all signal lines. It is proposed that all driver and termination information be removed from clause 5 and that additional notes be added to table 4 as needed to include all information being removed from clause 5.

#### 2. Timing

The logical signal definitions for DIOR, DIOW, RESET, and CSEL in clause 5 contain specific timing definitions. The description of the BSY bit in clause 7 contains specific timing information. The introduction to command descriptions in clause 8 contains specific timing information. The description portion of numerous commands contain specific timing information. It is proposed that all of these references be removed and that the clause 9, Protocol, and clause 10, Timing, be updated to insure that no removed timings are lost, e.g., add 400ns times in flow charts, add timing diagram showing valid RESET signal, etc.

#### 3. Protocols

In clause 9, the descriptions for many commands include a step by step description of the command protocol. It is recommended that these descriptions be removed (the protocol type in clause 9 is already referred to) and replaced by a simple description of what the command is used for. In the case of DEVICE RESET and EXECUTE DEVICE DIAGNOSTICS the commands are define as non-data commands and then a different protocol is described. It is recommended that these protocols be moved to clause 9 and that new protocol types be defined for them.

**Detailed changes:** Items accepted as written at the 8/21-23 meeting are preceeded by **A**, items modified at that meeting are preceeded by **M**, items added due to that meeting are preceeded by **N**.

**M** 4.3.1 Driver types and required termination - Table 4 - Add note 8 on PDIAG- "8 The host shall not drive the PDIAG- signal. If the host connects to the PDIAG- signal, the host shall ensure that the signal level seen on the interface for PDIAG- shall maintain  $V_{OH}$  and  $V_{OL}$  compatibility, given the  $I_{OH}$  and  $I_{OL}$  requirements of the PDIAG- device drivers." Add note 9 on DASP- "9 The host shall not drive the DASP- signal. If the host connects to the DASP- signal for any purpose, the host shall ensure that the signal level seen on the interface for DASP- shall maintain  $V_{OH}$  and  $V_{OL}$  compatibility, given the  $I_{OH}$  and  $I_{OL}$  requirements of the DASP- device drivers."

**A** 5.1 Signal summary - Add "For driver and termination definition see 4.3.1. For signal protocol and timing see clause 9 and clause 10."

**N** 5.2.1 and 5.2.2 CS0- and CS1- - Add “When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.”

**A** 5.2.4 DASP- - Delete “This signal shall be an open collector output and each device shall have a 10K $\Omega$  pull-up resistor. If the host connects to the DASP- signal for illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the interface for DASP- shall maintain  $V_{OH}$  and  $V_{OL}$  compatibility, given the  $I_{OH}$  and  $I_{OL}$  requirements of the DASP- device drivers.”

**N** 5.2.5 DD (15:0) - Add “Data transfers are 16-bits wide.”

**M** 5.2.6 DIOR- - Replace existing text with “ This is the strobe signal asserted by the host to read **device** registers or data port.”

**M** 5.2.7 DIOW- - Replace existing text with “ This is the strobe signal asserted by the host to write **device** registers or data port.”

**M** 5.2.9 DMARQ - Delete “This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.”

**A** 5.2.10 INTRQ - Replace existing text with “This signal is used by the selected device to interrupt the host system.”

**M** 5.2.12 IORDY - Delete “If actively asserted, this signal shall only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state. Add “This signal is negated to extend the host transfer cycle of any register read or write when the device is not able to complete the transfer.”

**A** 5.2.13 PDIAG- - Delete “A 10K $\Omega$  pull-up resistor shall be used on this signal by each device. The host shall not connect to the PDIAG- signal.”

**A** 5.2.14 RESET- - Replace text with “This signal, referred to as hardware reset, shall be used by the host to reset the device. See and .”

**A** 5.2.15 CSEL- - Delete “This signal shall have a 10K $\Omega$  pull-up resistor at each device.” Delete “CSEL shall be maintained at a steady level for at least 31 s after the negation of RESET-.”

**N** 7.1 Device addressing considerations - Add paragraph, “For register access protocol and timing see x.xx and y.yy.”

**A** 7.2.13 Status register - Delete “Note 5: Although host systems might be capable of generating read cycles shorter than the 400 ns specified for status update following the last command or data cycle, host implementations should wait at least 400 ns before reading the Status register to ensure that the BSY bit is valid.” In list items a) and b), delete the phrase “within 400 ns”.

**A** 8 Command descriptions - Delete “Upon receipt of a command, the device sets the BSY bit or the DRQ bit to one within 400 ns. Following the setting of the BSY bit to one, or the BSY bit to zero and the DRQ bit to one, the status presented by the device depends on the type of command: PIO data in, PIO data out, non-data transfer, DMA, PACKET command, overlap PACKET command data in, and overlap PACKET command data out.” Delete “Note 8: Some older host implementations may require the BSY bit being cleared to zero and the DRQ bit equal to one in the Status register within 700 ns of receiving some PIO data out commands.”

**A** 8.1.8 Description - Replace content with “The CHECK POWER MODE command allows the host to determine the current power mode of the device.”

**A** 8.2.3 Protocol - Replace “non-data” with “Device reset”

**A 8.2.8 Description** - Delete "Upon receipt of this command the device shall: a) Set BSY to one: b) Perform hardware initialization and diagnostics; c) May revert to its default condition; d) Post diagnostic results to the Error register; e) Clear BSY to zero."

**A 8.6.4 Protocol** - Replace "non-data" with "Device diagnostics".

**A 8.6.8 Description** - Delete content starting with the phrase " Device 0 performs the following .....".

**A 8.11.8 Description** - Replace the first sentence with "The IDLE command allows the host to place the device in the Idle Mode using the Standby Timer."

**A 8.12.8 Description** - Replace the first sentence with " The IDLE IMMEDIATE command allows the host to immediately place the device in the Idle Mode."

**M 8.13.8 Description** - Delete the second paragraph "Upon receipt of the command, the device sets the BSY bit to one, saves the parameters, clears the BSY bit to zero, and generates an interrupt." Replace the first sentence of paragraph three with "If the capacity of the device is less than 16,515,072 sectors, a device shall support the CHS translation described in words 1, 3, and 6 of the IDENTIFY DEVICE information."

**A 8.16.8 Description** - Delete the text "When this command is written to the Command register, the device sets BSY to one and prepares for the receipt of the command packet. When ready to receive the command packet, the device sets DRQ to one, sets C/D- to one, clears IO to zero, and clears BSY to zero. The device may assert INTRQ at this time but it is not recommended. The command packet is then transferred to the device via PIO transfer." Delete text "When the last word of the command packet is transferred, the device sets BSY to one and clears DRQ to zero."

**A 8.17.8 Description** - Delete text "When this command is issued, the device sets the BSY bit to one, sets up the sector buffer for a read operation, sets the DRQ bit to one, clears the BSY bit to zero, and generates an interrupt. The host then reads the data from the buffer."

**A 8.18.8 Description** - Replace existing text with "The READ DMA command allows the host to read device data using the DMA data transfer protocol."

**A 8.22.8 Description** - Delete second paragraph " When the requested sectors have been verified, the device clears the BSY bit to zero and generates an interrupt."

**A 8.33.8 Description** - Delete phrase "sets the BSY bit equal to one and".

**A 8.35.1.8 Description** - Delete paragraph "Upon receipt of the SMART DISABLE OPERATIONS command from the host, the device sets BSY to one, disables SMART capabilities and functions, clears BSY to zero and asserts INTRQ."

**A 8.35.2.8 Description** - Delete paragraph "If the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command is supported by the device, upon receipt of the command from the host, the device sets BSY to one, enables or disables the autosave feature (depending on the implementation), clears BSY to zero and asserts INTRQ."

**A 8.35.3.8 Description** - Delete the paragraph "Upon receipt of this command from the host, the device sets BSY to one, enables SMART capabilities and functions, clears BSY to zero and asserts INTRQ."

**A 8.35.4.8 Description** - Delete sentence "Upon receipt of this command from the host, the device sets BSY to one, reads the attribute thresholds from non-volatile memory, sets DRQ to one, clears BSY to zero, asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute threshold information from the device via the Data register."

**A 8.35.5.8 Description** - Delete sentence "Upon receipt of this command from the host, the device sets BSY to one, saves any updated attribute values to non-volatile memory, sets DRQ to one, clears BSY to zero,

asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute threshold information from the device via the Data register.”

**A** 8.35.6.8 Description - Delete sentence “Upon receipt of this command from the host, the device sets BSY to one, saves any updated attribute values to non-volatile memory and compares the updated attribute values to the attribute thresholds.”

**A** 8.35.7.8 Description - Delete sentence “Upon receipt of this command from the host, the device sets BSY to one, writes any updated attribute values to non-volatile memory, clears BSY to zero and asserts INTRQ.”

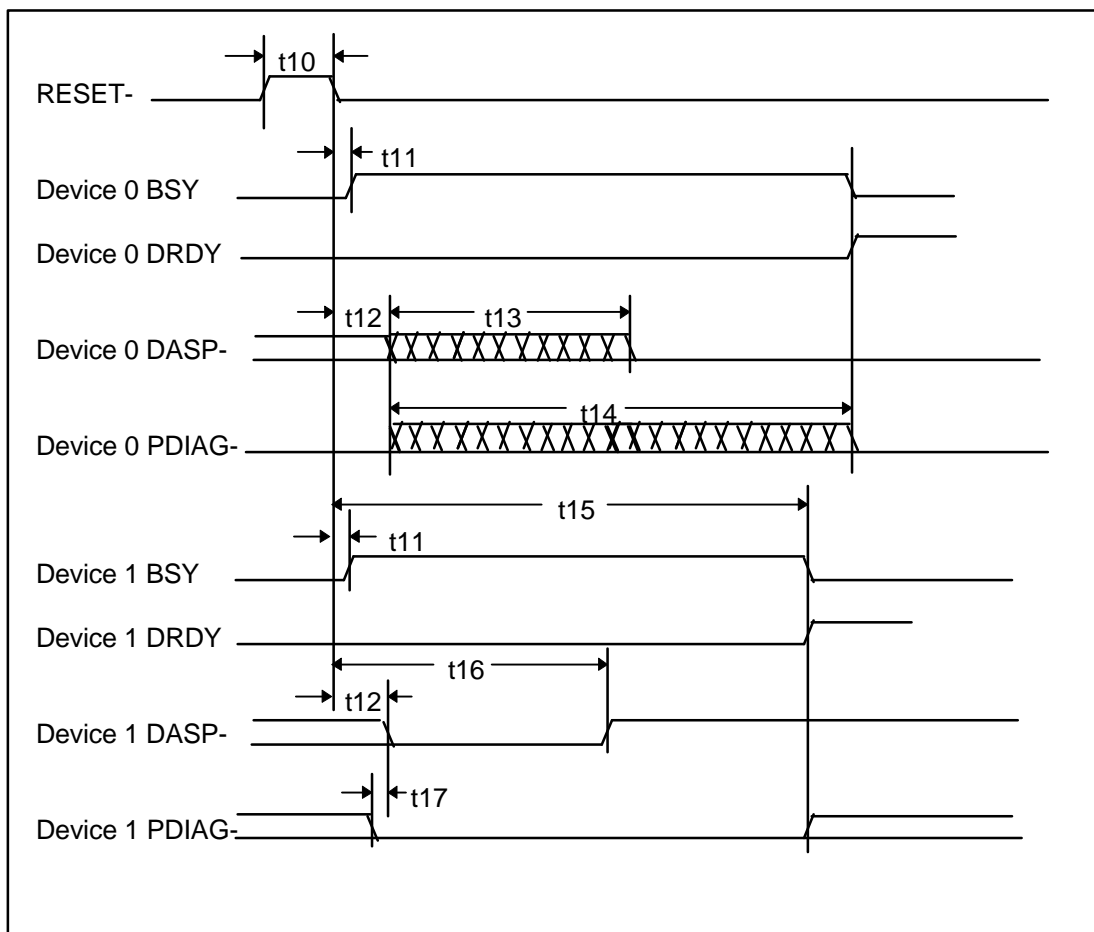
**A** 8.36.8 Description - Replace the first paragraph with “This command causes the device to enter the Standby mode.”

**A** 8.37.8 Description - Replace the first paragraph with “This command causes the device to immediately enter the Standby mode.”

**A** 8.38.8 Description - Delete text “When this command is issued, the device sets the BSY bit to one, sets up the buffer for a write operation, sets the DRQ bit to one, clears the BSY bit to zero, and generates an interrupt.”

**A** 8.39.8 Description - Replace existing text with “The WRITE DMA command allows the host to write device data using the DMA data transfer protocol.”

**M** 9.1 Power on and hardware resets - replace figure 8 with the following:



RESET timing parameters	Min	Max	Note
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t10	RESET pulsewidth	25 $\mu$ s		1
t11	RESET negation to BSY bit set to one		400 ns	
t12	DASP- and PDIAG- negation if asserted		1 ms	
t13	Device 0 sample of DASP-	1 ms	450 ms	2
t14	Device 0 sample of PDIAG-	1 ms	31 s	3
t15	Device 1 assert PDIAG-, clear BSY bit to zero		30 s	4
t16	Device 1 assert DASP-		400 ms	
t17	Device 1 negate PDIAG- if asserted	0 ns		

Notes:

1 The device shall not recognize a RESET assertion pulse width shorter than 20 ns as a valid signal assertion.

2 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until DASP- assertion by Device 1 is sensed or 450 ms has elapsed indicating no Device 1 present.

3 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until:

- no DASP- assertion is sensed in 450 ms,
- DASP- assertion is sensed in 450 ms and PDIAG- assertion is sensed,
- or DASP- assertion is sensed in 450 ms and no PDIAG- assertion is sensed in 31s.

When sampling is stopped, Device 0 shall clear the BSY bit to zero. DRDY shall be set to one when Device 0 is ready to accept any command. No maximum time is specified but a host should allow up to 30 s from the time RESET is negated.

4 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 30 s of the negation of RESET.

**M** 9.2 Software reset - enhance timing diagram as done above.

**M** After 9.2 Software reset - add in new protocol sections for Device reset and Device diagnostics by moving protocol description from existing command description.

**M** 9.3 through 9.7 - In flow charts in box "Device: Set BSY and begin command execution." add see note 1. Add note1 - "Host implementations shall/should wait at least 400 ns before reading the Status register to ensure that the BSY bit is valid."

**M** Table E.3 - Update protocol column for DEVICE RESET and EXECUTE DEVICE DIAGNOSTICS to reflect newly defined protocols.