

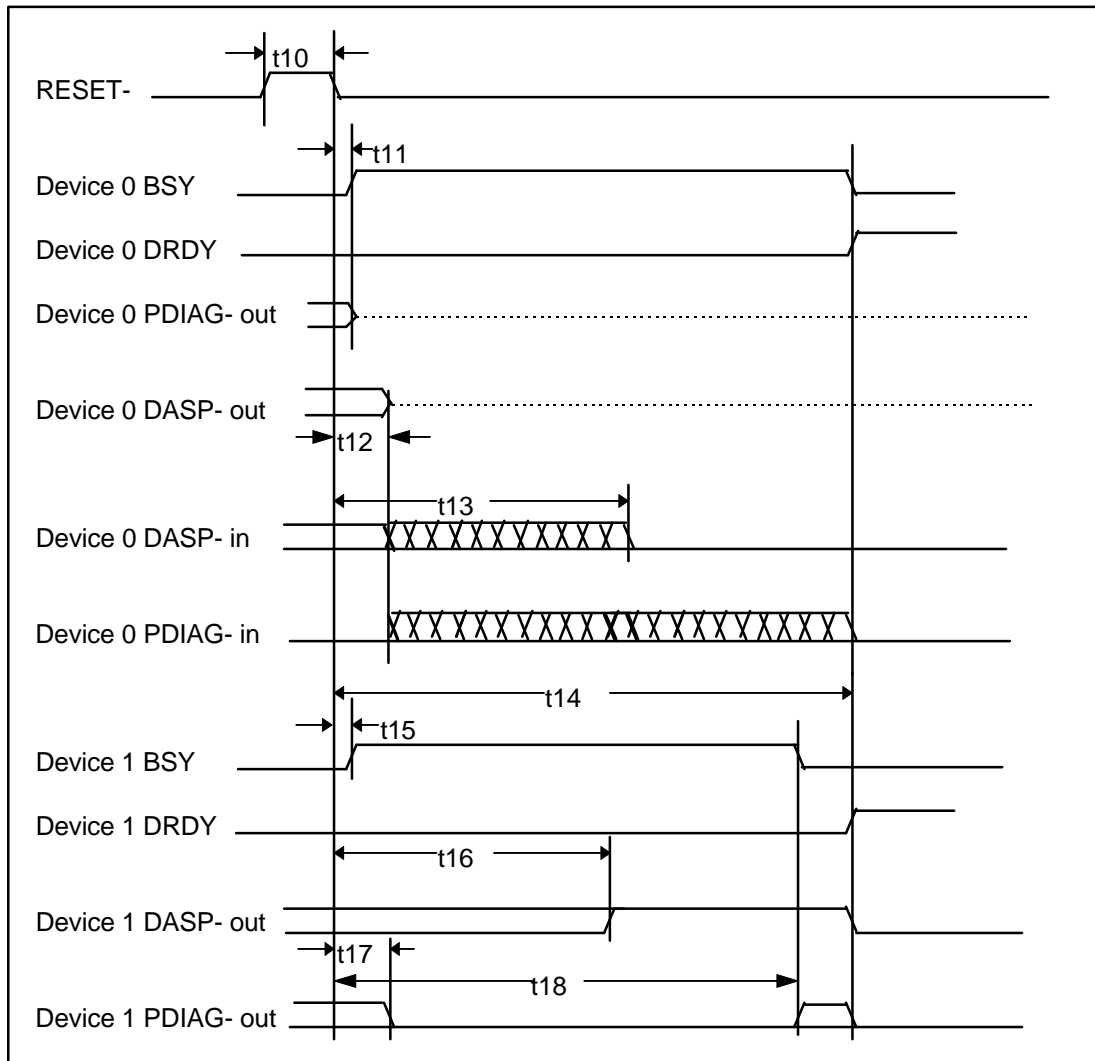
Proposal for removing redundant information in ATA/ATAPI-4

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Purpose: In many cases, the same items are specified in numerous locations throughout the document. In some cases, what is specified is in fact different in different locations. This proposal is intended to insure that each item is specified in only one location and that this location is the logical location for the specified material.

At the September 25-26 working group meeting, all of the content of D96114R1 was voted for inclusion into D1153R7, except the changes to timing diagrams. This revision contains only those timing diagrams.

8.1 Power on and hardware resets - replace figure 8 with the following:



RESET timing parameters		Min	Max	Note
t10	RESET pulsewidth	25 μ s		1
t11	Device 0 RESET negation to BSY bit set to one, release PDIAG-		400 ns	
t12	Device 0 release DASP-		1 ms	
t13	Device 0 sample of DASP-	1 ms	450 ms	2
t14	Device 0 sample of PDIAG-	1 ms	31 s	3
t15	Device 1 RESET negation to BSY bit set to one			
t16	Device 1 assert DASP-		400 ms	
t17	Device 1 negate PDIAG- if asserted		1 ms	
t18	Device 1 assert PDIAG-		30 s	4

Notes:

1 The device shall not recognize a RESET assertion pulse width shorter than 20 ns as a valid signal assertion.

2 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until DASP- assertion by Device 1 is sensed or 450 ms has elapsed indicating no Device 1 present.

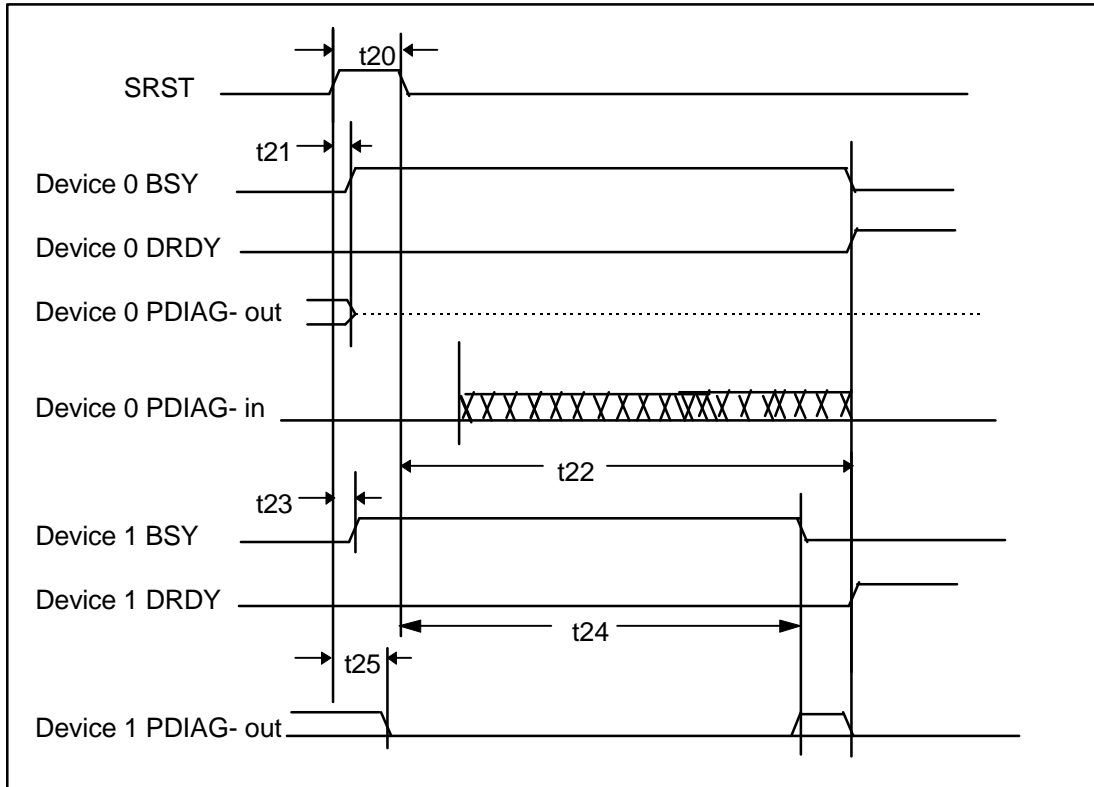
3 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until:

- no DASP- assertion is sensed in 450 ms,
- DASP- assertion is sensed in 450 ms and PDIAG- assertion is sensed,
- or DASP- assertion is sensed in 450 ms and no PDIAG- assertion is sensed in 31s.

When sampling is stopped, Device 0 shall clear the BSY bit to zero. DRDY shall be set to one when Device 0 is ready to accept any command. No maximum time is specified but a host should allow up to 30 s from the time RESET is negated.

4 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 30 s of the negation of RESET.

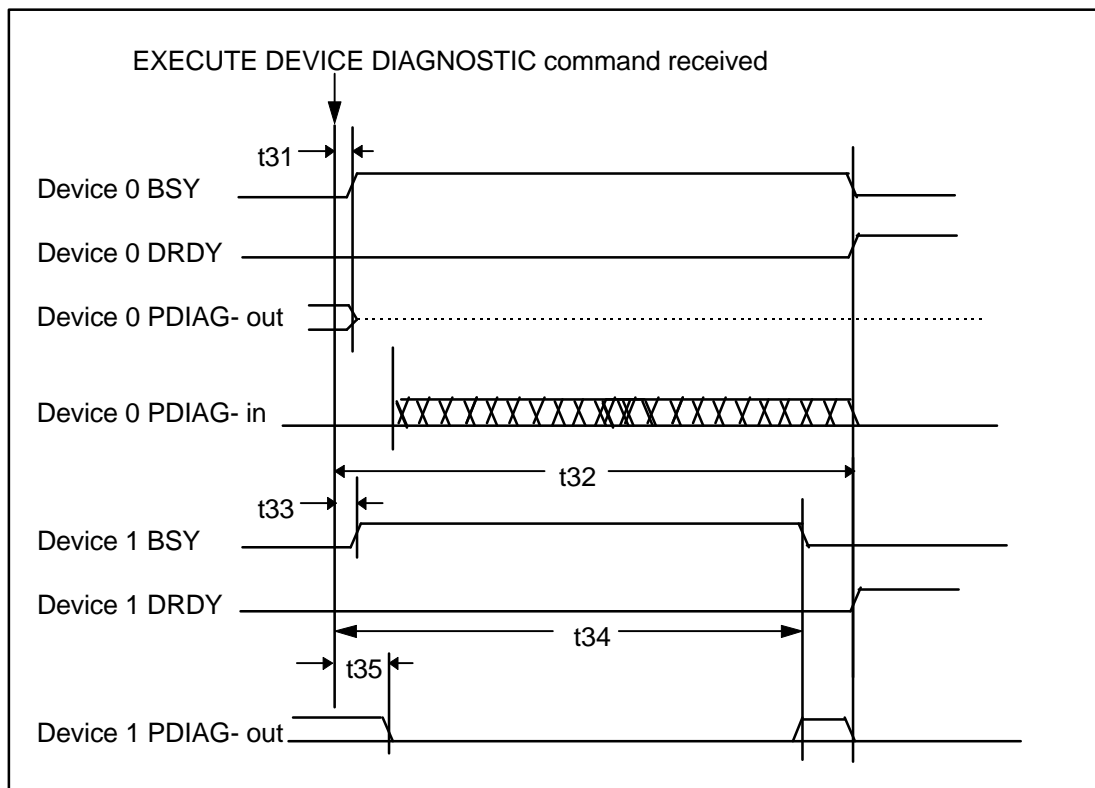
8.2 Software reset - replace figure 9 with the following:



SRST timing parameters		Min	Max	Note
t20	SRST bit set to one	5 μ s		
t21	Device 0 SRST set to one to BSY bit set to one, release PDIAG-		400 ns	
t22	Device 0 SRST cleared to zero to sample of PDIAG-	1 ms	31 s	1
t23	Device 1 SRST set to one to BSY set to one		400 ns	
t24	Device 1 SRST cleared to zero to BSY bit cleared to zero, PDIAG- asserted		30 s	2
t25	Device 1 negate PDIAG- if asserted		1 ms	

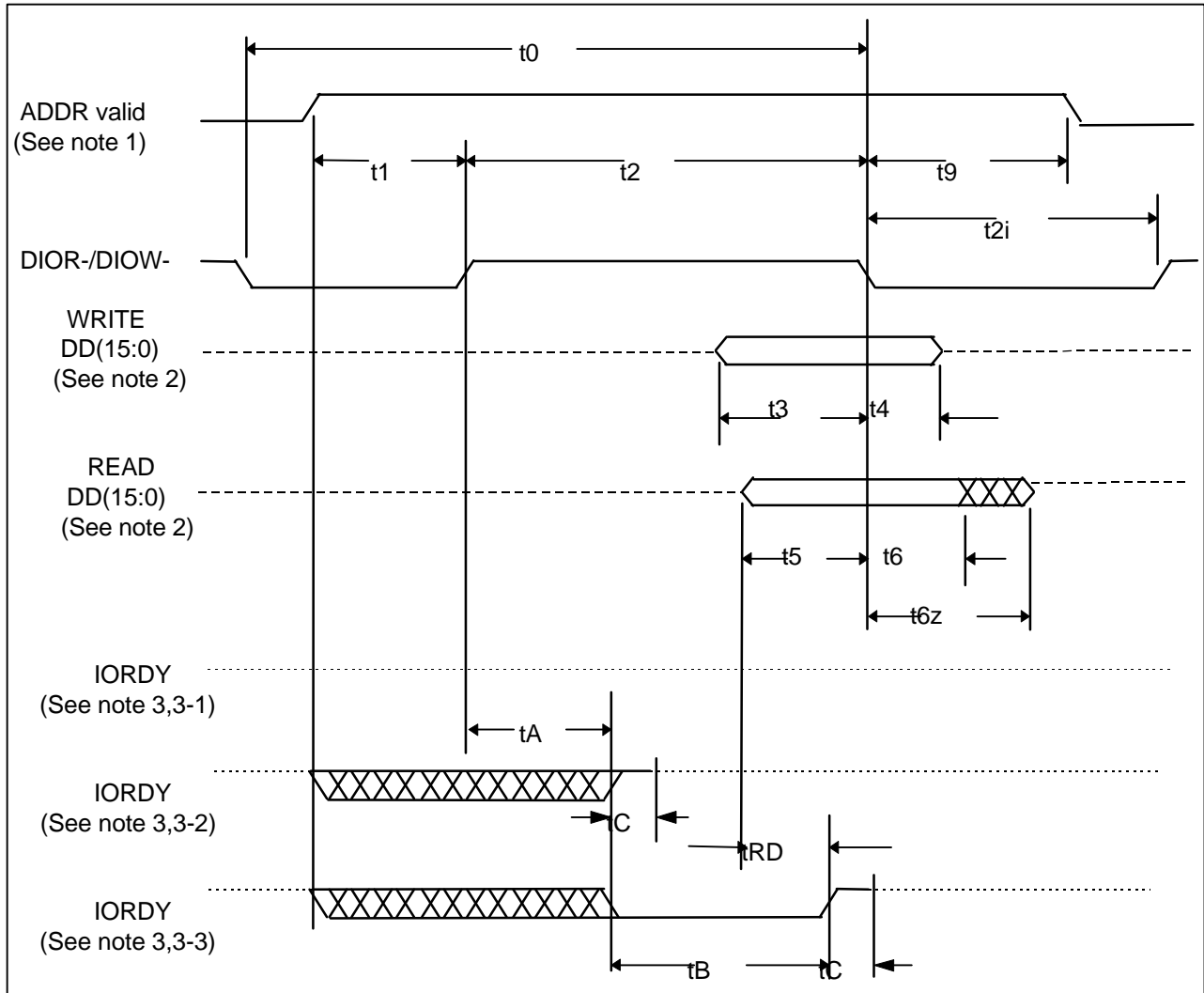
Notes:
 1 Device 0 shall sample beginning 1 ms after SRST is cleared to zero. Sampling shall continue until PDIAG- assertion by Device 1 is sensed or 31 s has elapsed indicating Device 1 failed diagnostic.
 2 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 30 s of the SRST being cleared to zero.

8.3 Device diagnostic protocol- replace figure 10 with the following:



EXECUTE DEVICE DIAGNOSTIC timing parameters		Min	Max	Note
t31	Device 0 command received to BSY bit set to one, release PDIAG-		400 ns	
t32	Device 0 command received to sample of PDIAG-	1 ms	6 s	1
t33	Device 1 command received to BSY set to one		400 ns	
t34	Device 1 command received to BSY bit cleared to zero, PDIAG- asserted		5 s	2
t35	Device 1 negate PDIAG- if asserted		1 ms	

Notes:
 1 Device 0 shall sample beginning 1 ms after receipt of the command. Sampling shall continue until PDIAG- assertion by Device 1 is sensed or 6 s has elapsed indicating Device 1 failed diagnostic.
 2 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 5 s of the receipt of the command.



Notes:

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(15:0).

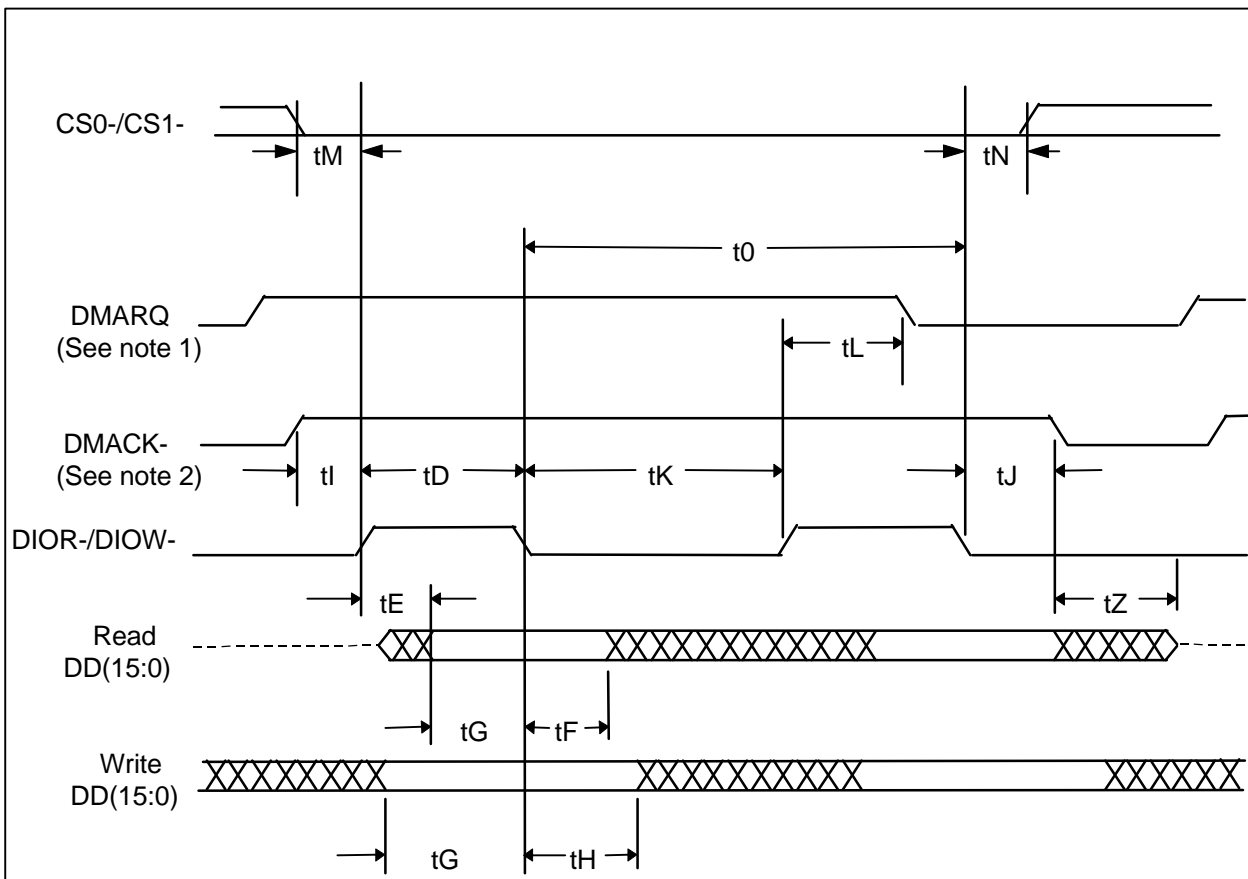
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY, device keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before t_A , but causes IORDY to be asserted before t_A . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.

3-3 Device negates IORDY before t_A . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted.

For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for t_{RD} before asserting IORDY.



NOTE:

- 1 For Multi-Word DMA transfers, the Device may negate DMARQ within the t_L specified time once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK-.
- 2 This signal may be negated by the Host to suspend the DMA transfer in process.