

Editor's ommision in ATA-3 (X3T13/D2008r7)

Pete McLean
Maxtor Corporation
2190 Miller Drive
Longmont, CO 80501
303 678-2149
pete_mclean@maxtor.com

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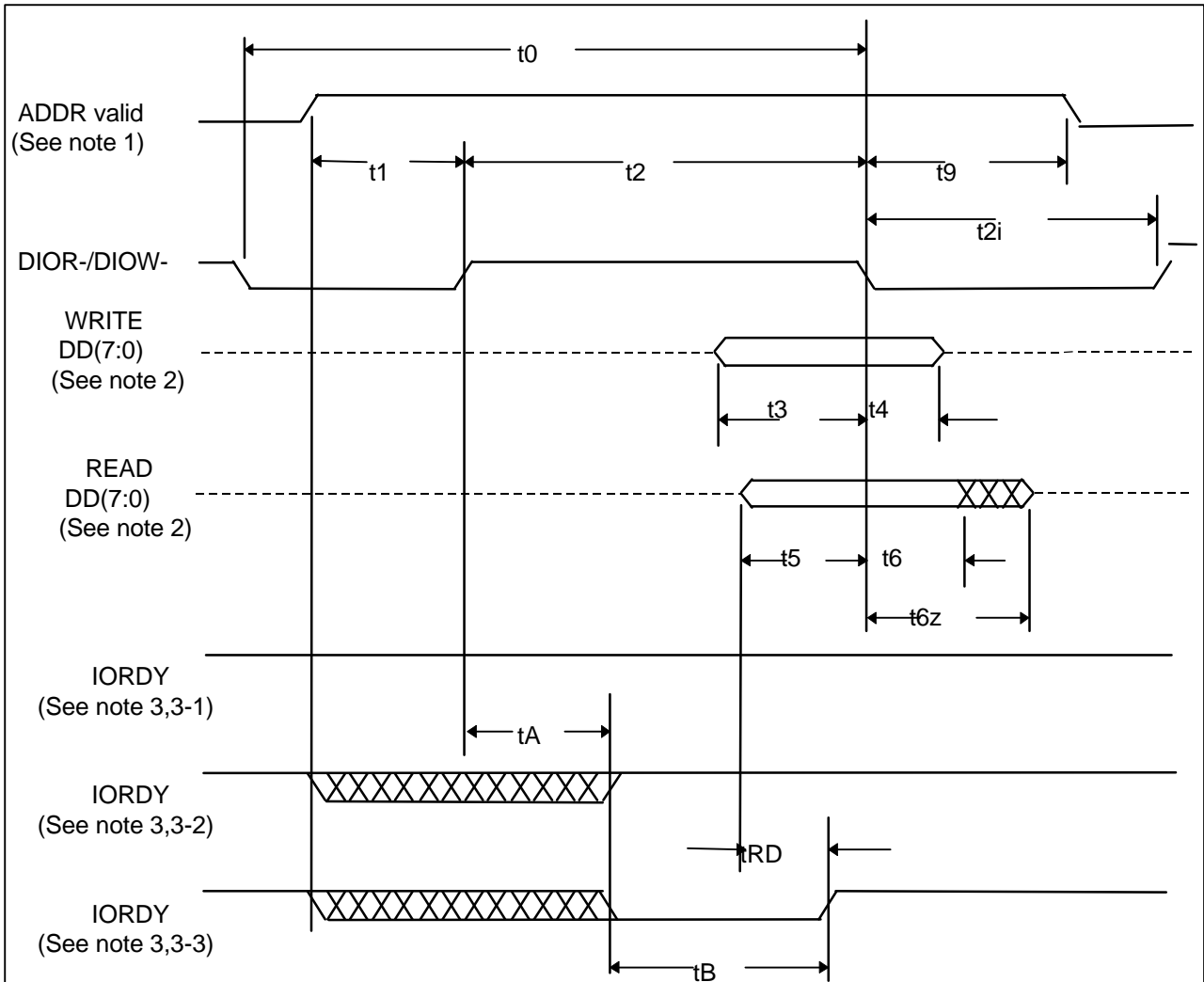
It was pointed out at the June 19-21, 1996 ad hoc meetings that when I removed 8-bit data transfers from the ATA-3 document, I also inadvertently removed timing for 8-bit register reads and writes. It is proposed that the following clause be added to rectify this editorial mistake and return the required definition to the ATA-3 document.

10.4.1 Register transfers

Figure 14 defines the relationships between the interface signals for 8-bit PIO register transfers. This timing applies to all register accesses except accesses to the Data register. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the Identify Drive parameter list. Table 22 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.



NOTES –

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(7:0).

3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY: no wait is generated.

3-2 Device negates IORDY before t_A , but causes IORDY to be asserted before t_A : no wait generated.

3-3 Device negates IORDY before t_A : wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

Figure 14– Register transfer to/from device

Table 22 – Register transfer to/from device

PIO timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t0	Cycle time (min)	600	383	240	180	120	1
t1	Address valid to DIOR-/DIOW- setup (min)	70	50	30	30	25	
t2	DIOR-/DIOW- 8-bit (min)	290	290	290	80	70	1
t2i	DIOR-/DIOW- recovery time (min)	-	-	-	70	25	1
t3	DIOW- data setup (min)	60	45	30	30	20	
t4	DIOW- data hold (min)	30	20	15	10	10	
t5	DIOR- data setup (min)	50	35	20	20	20	
t6	DIOR- data hold (min)	5	5	5	5	5	
t6Z	DIOR- data tristate (max)	30	30	30	30	30	2
t9	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	
tRd	Read Data Valid to IORDY active (if IORDY initially low after tA)	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	

NOTES –

1 t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify drive data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.