T13/D97121R0

Proposal for inclusion of additions to ATA/ATAPI-4 required to specify an 80-conductor cable assembly and a 40-conductor cable assembly with an alternate CSEL configuration

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Subj: **Proposal for inclusion of additions to ATA/ATAPI-4 required to specify an 80-conductor cable assembly**

Introduction:

The following is a proposal for inclusion into ATA/ATAPI-4 of elements required to define an 80-conductor ATA interface cable assembly. This cable uses the same connectors as specified for the standard 40-conductor ATA cable, but has an additional 40 ground lines alternating with the defined 40 signal lines for improvement in signal quality. In addition, this proposal includes the revisions necessary to describe a 40-conductor cable assembly where CSEL is connected in such a way as to provide for a configuration where Device 0 is at the opposite end of the cable from the host. This proposal is designed as a “drop-in” to ATA/ATAPI-4 and is based on D1153r11.

2.3 Other references

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[add the following]

80-conductor ATA Cable Assembly [SFF-8049]

4.2 I/O cable

The cable specification affects system integrity and the maximum length that shall be supported in any application.

Cable total length shall not exceed 0.46 m (18 in).

Cable capacitance shall not exceed 35 pf.

[Do we need to say anything else here?]

4.3.1 Driver types and required termination

Table 4 - Driver types and required termination

Signal	Source	Driver type (see note 1)	Host (see note 2)	Device (see note 2)	Notes
RESET	Host	TP			
DD (15:0)	Bidir	TS			3
DMARQ	Device	TS	5.6 kΩ PD		4
DIOR-:HDMARDY-:HSTROBE	Host	TS			
DIOW-:STOP	Host	TS			
IORDY:DDMARDY-:DSTROBE	Device	TS	1.0 kΩ		7
CSEL	Host		Ground	10 kΩ	5, 7
DMACK-	Host	TP			
INTRQ	Device	TS			6
DA (2:0)	Host	TP			
PDIAG-:CBLID-	Device	TS		10 kΩ	7, 8, 9
CS0- CS1-	Host	TP			
DASP-	Device	OC		10 kΩ	7, 10

Notes:
1 TS=Tri-state; OC=Open Collector; TP=Totem-pole; PU=Pull-up; PD=Pull-down
2 All resistor values are the minimum (lowest) allowed.
3 Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in a future revision of this standard.
4 DMARQ shall be driven from its first assertion at the beginning of a DMA transfer until it is negated after the last word is transferred. This signal shall be tri-stated at all other times.
5 When used as CSEL, this line is grounded at the host and a 10 kΩ pull-up is required at both devices.
6 If the host uses a level sensitive interrupt controller a 10k pull-down or pull-up, depending upon the level sensed, may be required at the host.
7 Pull-up values are based on +5 v Vcc.
8 The host shall not connect to PDIAG-.
9 CBLID shall be grounded in the host connector for 80-conductor cable assemblies.
10 The host shall not drive DASP- . If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain V_{oH} and V_{oL} compatibility, given the I_{oH} and I_{oL} requirements of the DASP- device drivers.

5.1 Signal summary

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Table 6 – Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select	(see note)			CSEL
Chip select 0			→	CS0-
Chip select 1			→	CS1-
Data bus bit 0		↔		DD0
Data bus bit 1		↔		DD1
Data bus bit 2		↔		DD2
Data bus bit 3		↔		DD3
Data bus bit 4		↔		DD4
Data bus bit 5		↔		DD5
Data bus bit 6		↔		DD6
Data bus bit 7		↔		DD7
Data bus bit 8		↔		DD8
Data bus bit 9		↔		DD9
Data bus bit 10		↔		DD10
Data bus bit 11		↔		DD11
Data bus bit 12		↔		DD12
Data bus bit 13		↔		DD13
Data bus bit 14		↔		DD14
Data bus bit 15		↔		DD15
Device active or slave (Device 1) present	(see note)			DASP-
Device address bit 0			→	DA0
Device address bit 1			→	DA1
Device address bit 2			→	DA2
DMA acknowledge			→	DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read DMA ready during Ultra DMA data in bursts Data strobe during Ultra DMA data out bursts			→ → →	DIOR- HDMARDY- HSTROBE
I/O ready DMA ready during Ultra DMA data out bursts Data strobe during Ultra DMA data in bursts	← ← ←			IORDY DDMARDY- DSTROBE
I/O write Stop during Ultra DMA data bursts			→ →	DIOW- STOP
Passed diagnostics Cable assembly type identifier	(see note) (see note)			PDIAG- CBLID
Reset			→	RESET-
NOTE – See signal descriptions for information on source of these signals				

5.2.11 PDIAG–/CBLID– (Passed diagnostics/Cable assembly type identifier)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed its self-diagnostic testing.

The host may sample this signal after the completion of each hardware reset sequence in order to detect the presence or absence of an 80-conductor assembly. If the host detects that the signal is connected to ground, then an 80-conductor assembly is installed in the system. If the host detects that the signal is not is connected to ground, then an 80-conductor assembly is not installed in the system.

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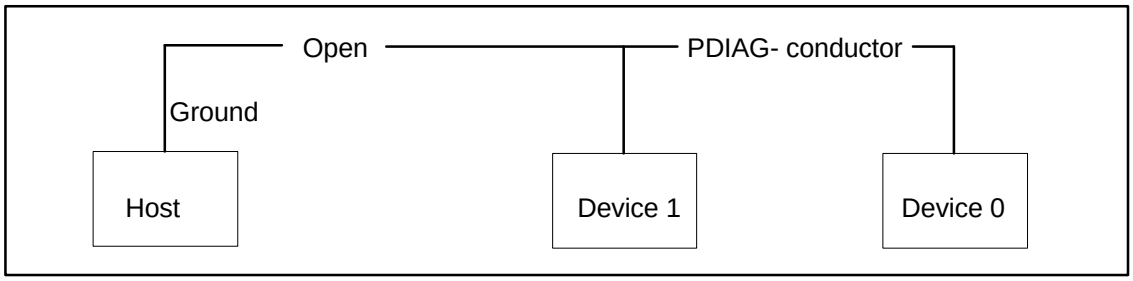

Figure x1 – PDIAG– example using an 80-conductor cable assembly

5.2.13 CSEL (Cable select)

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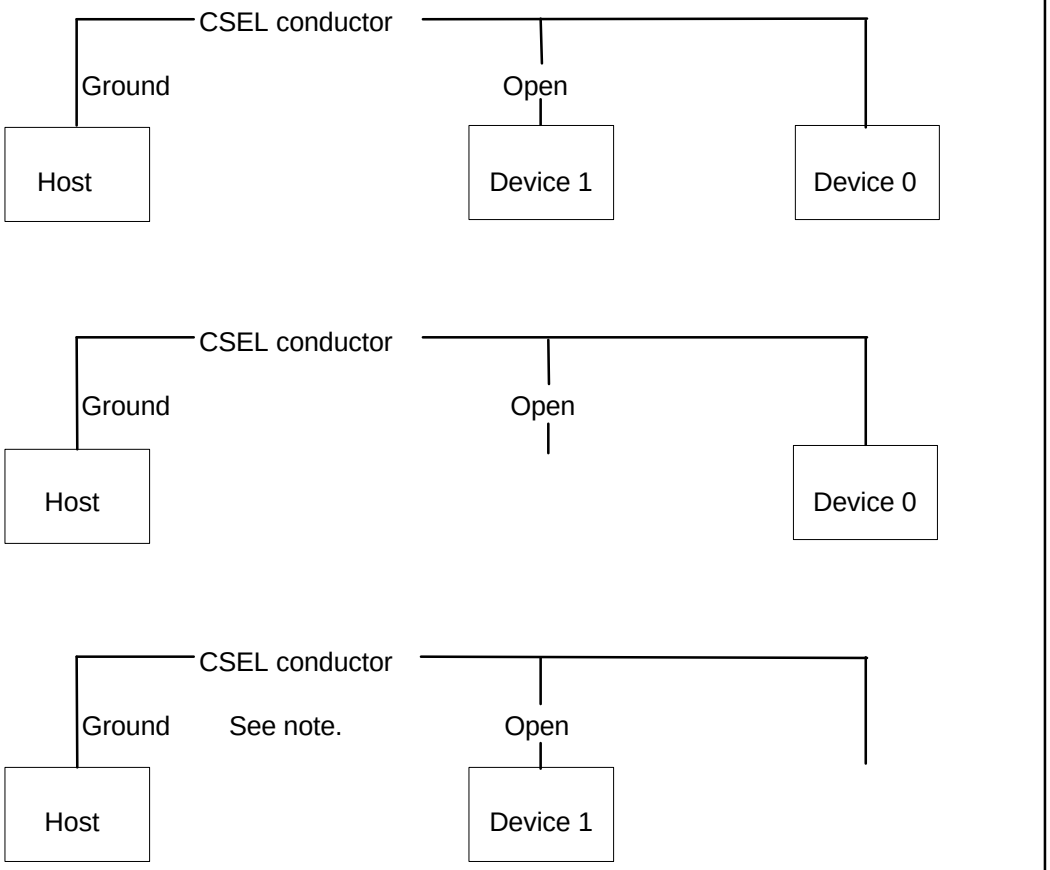
NOTE – For designated cable assemblies (including all 80-conductor cable assemblies): these assemblies are constructed so that CSEL is connected from the host connector to the connector at the opposite end of the cable from the host. Therefore, Device 0 shall always be at the opposite end of the cable from the host. It should be recognized that if a single device is configured at the connector not at end of the cable a Device 1 only configuration results.



NOTE – If a single device configuration is implemented with the device in the middle of the cable assembly, a cable stub results that may cause degradation of signals.

Figure x2 – Alternate cable select example

Annex A
(normative)
Connectors

[The following clause shall be added in this annex.]

A.x 40-pin connector using an 80-conductor cable

The I/O connector is a 40-pin connector as shown in figure A.1. However, for this assembly, an 80-conductor ribbon cable is used where all of the even conductors are tied to ground in order to improve signal integrity. Pin assignments for this assembly are shown in table A.x. The connector shall be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20 from the device and host connectors. The corresponding pin on the cable connector shall be plugged.

The connector contact for CBLID– shall be connected to ground in the connector for the host. The conductor for PDIAG– shall not be connected to the connector contact for CBLID– in the connector for the host.

CSEL shall not be connected to the connectors at the ends of the cable. If a connector is present in the middle of the cable, then CSEL shall not be connected to this connector.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, that is keyed.

By using the plug positions as primary, a straight cable connects devices. As shown in figure A.1, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

Table A.x – 40-pin connector interface signals using 80-conductor cable

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	3	2	Ground
DD7	3	5	7	4	DD8
DD6	5	9	11	6	DD9
DD5	7	13	15	8	DD10
DD4	9	17	19	10	DD11
DD3	11	21	23	12	DD12
DD2	13	25	27	14	DD13
DD1	15	29	31	16	DD14
DD0	17	33	35	18	DD15
Ground	19	37	39	20	(keypin)
DMARQ	21	41	43	22	Ground
DIOW-:STOP	23	45	47	24	Ground
DIOR-:HDMARDY-:HSTROBE	25	49	51	26	Ground
IORDY:DDMARDY-:DSTROBE	27	53	55	28	CSEL (see note 2)
DMACK-	29	57	59	30	Ground
INTRQ	31	61	63	32	reserved
DA1	33	65	67	34	PDIAG-:CBLID- (see note 3)
DA0	35	69	71	36	DA2
CS0-	37	73	75	38	CS1-
DASP-	39	77	79	40	Ground

Notes:
1) All even-numbered conductors are connected to ground inside each of the connectors.
2) In a cable assembly providing connectors for two devices and a host conductor 55 shall not be connected to connector contact 28 in the connector in the middle position. This configuration results in Device 0 being at the opposite end of the cable from the host.
3) Connector contact 34 in the connector for the host shall be connected to ground. Conductor 67 shall not be connected to connector contact 34 in the connector for the host.