ATA/100

Eric Kvamme

Quantum Corporation

Manager, Desktop Interface Engineering

(408) 894-6478

eric.kvamme@quantum.com

Agenda

- **ATA/100 goals**
- **What was done to meet goals**
- **Recommendations for testing and example results**
- **Recent change to mode 5 t_{DVS}, t_{DVH} timing listed in table**
  - Not a change in hardware timing requirement
- **Run through of ATA/100 rev 2 specification**

ATA/100 Goals

- **Increase transfer rate to 100MB/s**
- **Maintain uniform implementation of ATA interface**
- **No change in cabling or connectors**
- **No decrease in reliability (design for no CRC errors)**
- **Resolve reliability issues seen on ATA/66 designs**
  - Resolve signal integrity problems and mistakes seen on ATA/66.
  - Clarify timing definitions and margin to avoid timing errors seen with ATA/66.

Cable Length

- **Shorter cabling not required for ATA/100.**
  - Skews at the middle connector are primarily dependant on it's distance from the end of the cable, increasing an 80 conductor cable length from 1.5" to 18" adds only about 400ps of skew. This is less than 15% of the IC pin to IC pin timing budget.
  - Conductors of 80 conductor cable account for less than 20% of crosstalk in systems measured to date. Most crosstalk is generated in the source traces and connector so cable length from 1.5" to 18" not a significant factor in crosstalk level.
  - Shorter cables not required but can be used to improve timing margin and reduce crosstalk.
- **Interlock timings and skew budget account for 18" cable - no change to current ATA/66 cable.**
- **longer cables not recommended.**

Reliability Issues

- **To date, transfer errors have been seen on ATA/66 systems that typically meet the ATA/66 electrical and timing specification for the following reasons:**
  - Slew rate and noise sensitivity on STROBE due to no hysteresis.
  - High output impedance and 5V signaling resulting in a falling edge where the incident edge and first reflection does not cross V-.
  - Too low output impedance leading to large ringing and reflections.
  - High crosstalk leading to 0 strobed as 1 (in conjunction with a device that has a low V+ threshold).
  - First word timing violations.
  - Insufficient typical setup or hold time.
  - IC level crosstalk (ground bounce) during data transfer.
  - Logic errors

Reliability/Slew Rate Sensitivity

- **Some ATA/33 and ATA/66 hosts have been shown to be sensitive to slew rate and noise due to lack of hysteresis on the STROBE input.**
- **Result is CRC errors which are independent of Ultra DMA mode.**
- **Hysteresis requirement added in ATA/100 specification.**
  - Minimum hysteresis of 320mV. Sufficient for noise levels seen in Ultra DMA systems to date.
  - When process, temperature, and voltage variations are considered typical hysteresis is over 500mV.
  - Higher value minimum not possible with other threshold requirements.

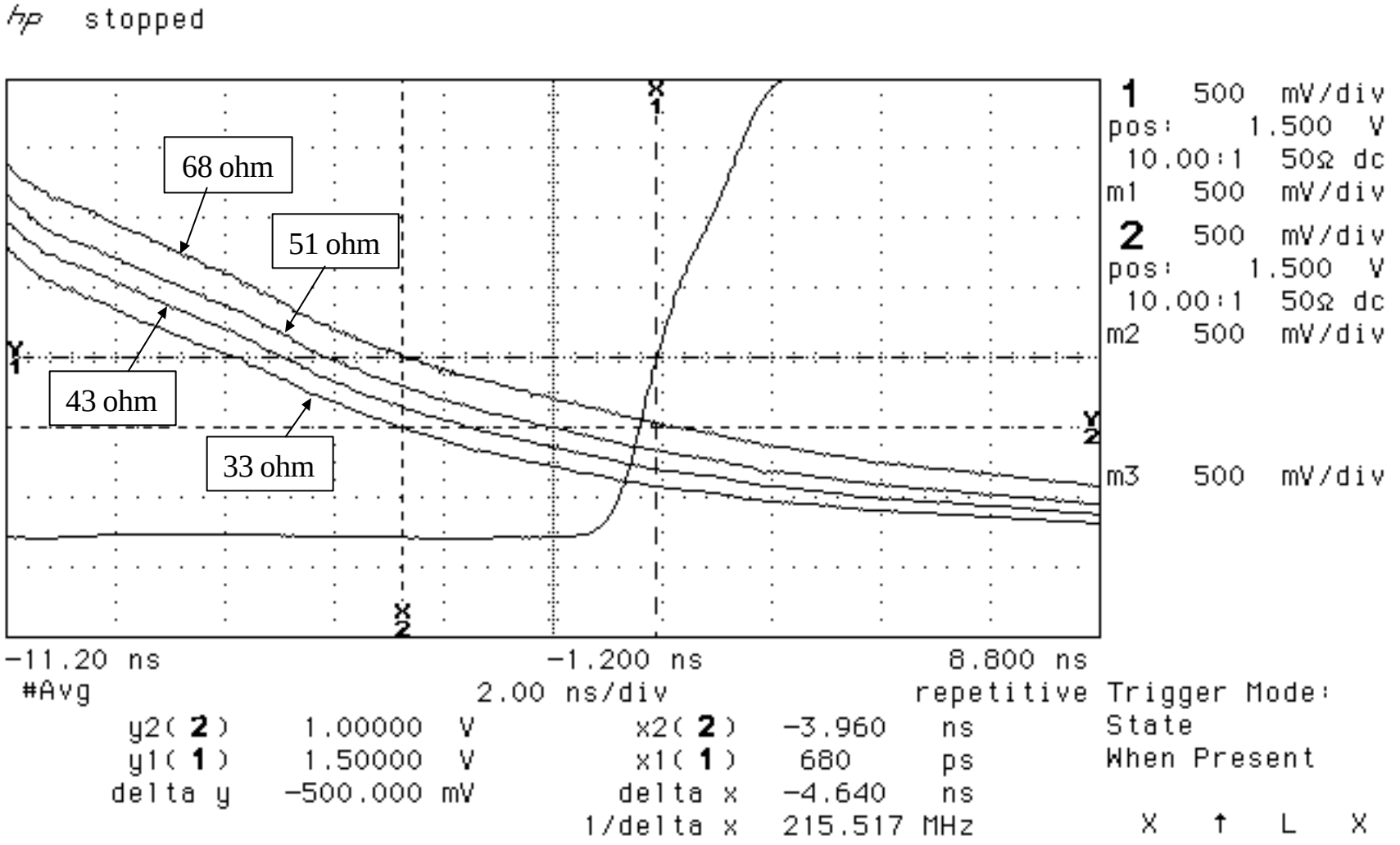
Reliability/High Output Impedance

Desktop Interface Engineering

- **High output impedance with a 5V Voh can lead to a falling edge that doesn't cross the threshold until long after the edge crosses 1.5V.**
- **CRC errors generated only in fastest mode.**
- **ATA/100 requires 3.3V signaling only from sender and receiver.**
  - Pull up and pull down resistors to 3.3V.
  - Voh has min and max around 3.3 which must be met at both positive and negative current (while being pulled up or down).
- **ATA/100 has min and max resistance for output on resistance + series termination value.**
  - Maximum total output resistance value and 3.3V signaling guarantees that input signal will cross the V- or V+ threshold on the incident edge with it's reflection.

High Output Impedance Waveform

Desktop Interface Engineering



Reliability/High Crosstalk

- **An obvious source of some CRC errors is crosstalk.**
- **As with ringing, Crosstalk typically settles fast enough for the slower modes so only the highest modes are affected.**
- **Crosstalk can come from a number of sources including:**
  - Fast slew rates (dV/dt)
  - Fast changes in output current (di/dt) during a transition
  - Layouts with traces that are parallel and closely spaced for a long distance.
  - The use of a right angle through hole connector

Reliability/High Crosstalk

- **A new specification (V_{SSO}) was added which will for the most part limit total crosstalk to an acceptable level while still allowing for some design flexibility (an NLX system with long but well spaced traces for example).**
- **Crosstalk for the system should not exceed 800mV when both V_{SSO} and the slew rate specification are met.**
  - Crosstalk this low is not actually a requirement for ATA/100 receivers due to the new threshold specifications.
  - Some legacy devices do require this restricted crosstalk so it is being added to the general AC requirements.
- **Higher V_{SSO} allowed at the Host (600mV) compared to the device (500mV).**
  - Typical host has longer traces and accounts for more of crosstalk budget.

Reliability/High Crosstalk

- **Even with High Crosstalk, a system can work properly with thresholds far enough from Vol and Voh.**
  - ATA/66 CRC errors which resulted from high crosstalk occurred with receiving thresholds that were biased closer to Vol.
  - High crosstalk does not result in CRC errors if the receiving threshold is further from Vol or Voh than the peak crosstalk.
- **Specification added for V+ and V-**
  - Minimum V+ defined at 1.5V to allow for crosstalk at Vol.
  - Maximum V- defined at 1.5V to allow for crosstalk at Voh.
- **New V+ and V- specifications allow error free transfers with more crosstalk than observed on ATA/66 systems.**

Reliability/IC Level Crosstalk

- **High supply (power or ground) bounce in a chip while receiving data can result in the wrong value of that data being observed.**
  - This type of problem has been seen on an ATA/33 chip.
  - The new input threshold levels with hysteresis give more margin for this type of bounce
- **High supply bounce or crosstalk in a chip while sending data can result in the wrong value being sent.**
  - Typically the supply bounce settles quickly and in that case only affects the higher modes.
  - IC level crosstalk that occurs while data is being strobed could result in error in any mode.
  - The V_{SSO} specification limits both forms of bounce/crosstalk while outputting to a level which should not cause transfer errors.

Reliability/Timing Budget

Desktop Interface Engineering

- **ATA/66 gave all timings at the connectors.**
  - Confusion about which connector to use to measure some timings.
  - Assumes layout guidelines are followed (not always true).
  - Not valid to measure t_{DVS} and t_{DVH} in a cabled system due to reflections that change the sender observed timing.
  - Not clear what timing budget is for ICs.
- **ATA/100 Solutions:**
  - New column added defining exactly which connector to use.
  - Trace Length variation defined.
  - Min and max range for on resistance plus termination bounds design window and tightens IC to IC skew.
  - ATA/100 refines source side setup/hold into lumped loads. No change to interlocks and other non-critical timings that already accounted for reflections in functioning system.
  - Setup and hold timings at source and recipient IC pins added.

Reliability/First Word Timing Violation

- **A 5V legacy device may be present on the cable.**
  - When the bus is not driven, the 5V device may have bias current which pulls the bus to 5V.
  - On the first DATA and STROBE edges, the fall times and settle times may be longer if the output is enabled to to generate the edge or enabled too soon before the edge.
  - The ATA/66 specification had sufficient output skew margin to allow for some additional first word skews, ATA/100 doesn't.
- **ATA/100 Solutions:**
  - Voh min/max requires I/O to pull up or down to 3.3V when high.
  - New timing parameters require all outputs to be enabled with sufficient time before the first critical timing edge for the I/O to settle and to pull the bus to the proper output voltage.
  - Proper starting output voltage and sufficient I/O settling time results in adequate first word timing.

Slew Rate Testing

- **Slew rate may be testing in a non-destructive way.**
  - Requires modifications to a standard 80-conductor cable.
  - Requires switching from one connector to another on the same cable at the source under test or requires hot swapping the entire cable after setup.
    - Signal under test on test cable is open on cable.
    - System will not boot with test cable in place.
  - Requires test software that can control data patterns and deal with CRC errors.
- **For host systems with long PCB traces, slew rates measured at the connector may not be a precise representation of the slew rate generated by the IC and seen at the recipient.**
  - The specification does allow for destructive testing of these systems to more precisely determine the IC characteristics.

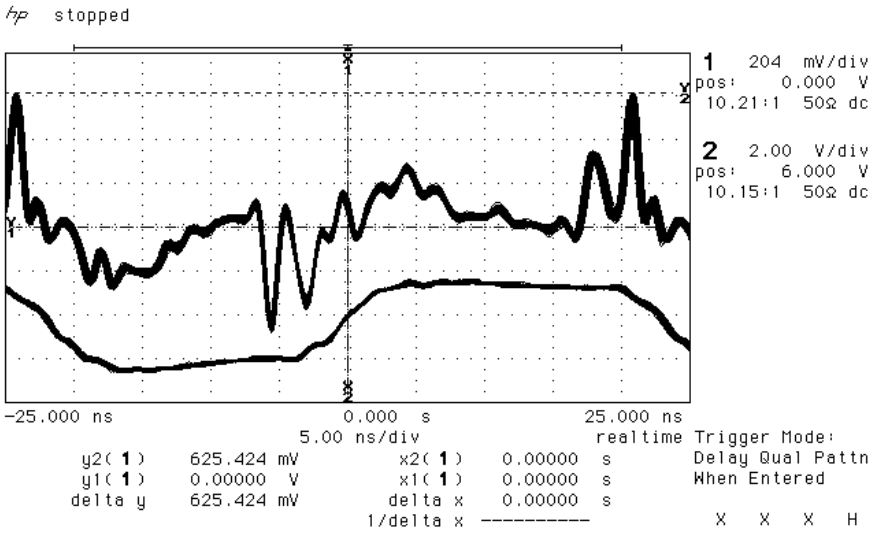
V_{SSO} Testing

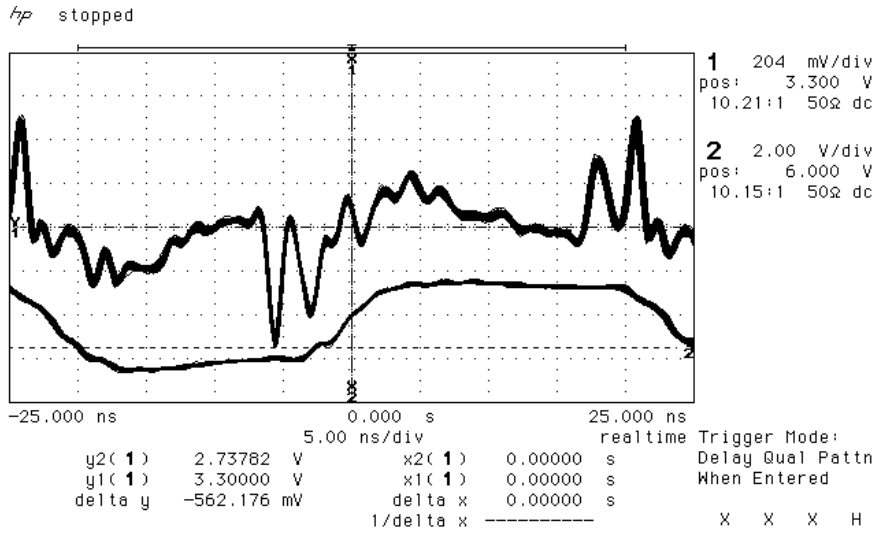
- **V_{SSO} must be tested at the source connector as defined in order to include crosstalk in connector.**
  - Requires modifications to a standard 80-conductor cable.
  - Requires switching from one connector to another on the same cable at the source under test or requires hot swapping the entire cable after setup.
    - Signal under test on test cable is open on cable.
    - System will not boot with test cable in place.
  - Requires test software that can control data patterns and deal with CRC errors.

V_{HSSO} with ATA/100 host

Desktop Interface Engineering

Port	Description	Max specification (mV)	Max negative delta from DC output (mV)	Max Positive V_{HSSO} (mV)	Figure
Primary	DD12 at Vol	600		625	5
	DD12 at Voh	-600 from DC Voh	-562		6
	DD15at Vol	600		396	7
	DD15 at Voh	-600 from DC Voh	-383		8





V_{DSSO} with Quantum ATA/100 interface

Desktop Interface Engineering

Description	Max specification (mV)	Max negative delta from DC output (mV)	Max Positive V_{DSSO} (mV)	Figure
DD12 at Vol	500		286	2
DD12 at Voh	-500 from DC Voh	-191		3
DD15at Vol	500		172	-
DD15 at Voh	-500 from DC Voh	-121		-

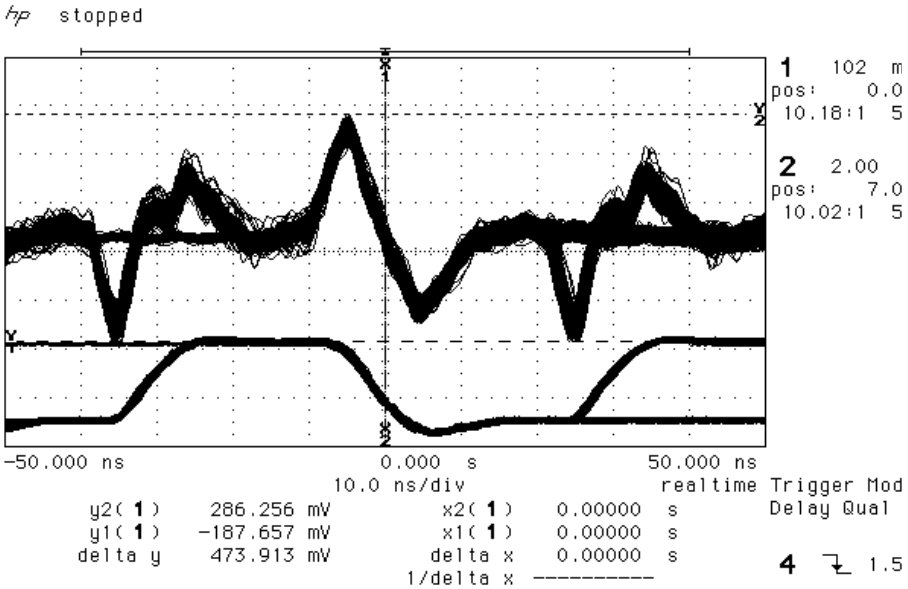


Figure 2: DD12 @ Vol

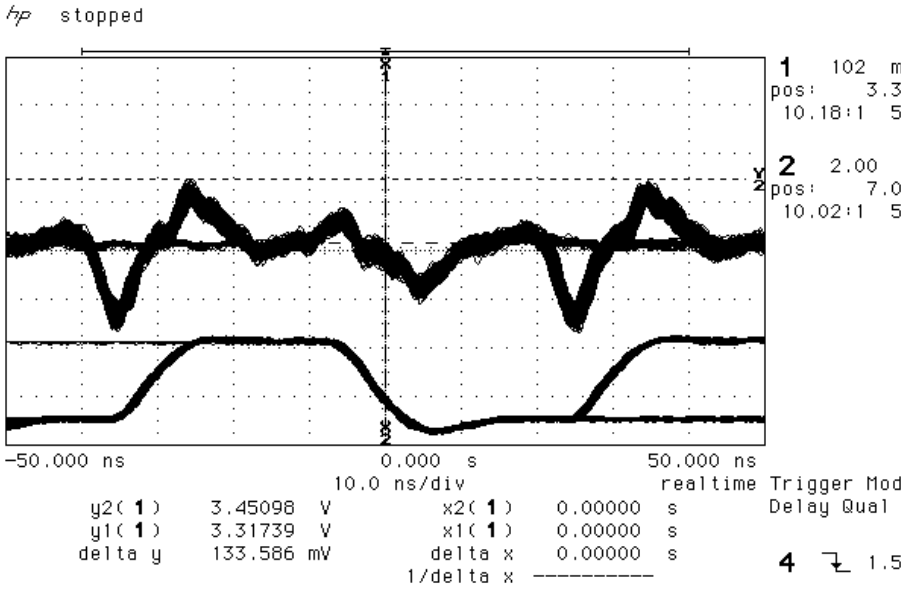
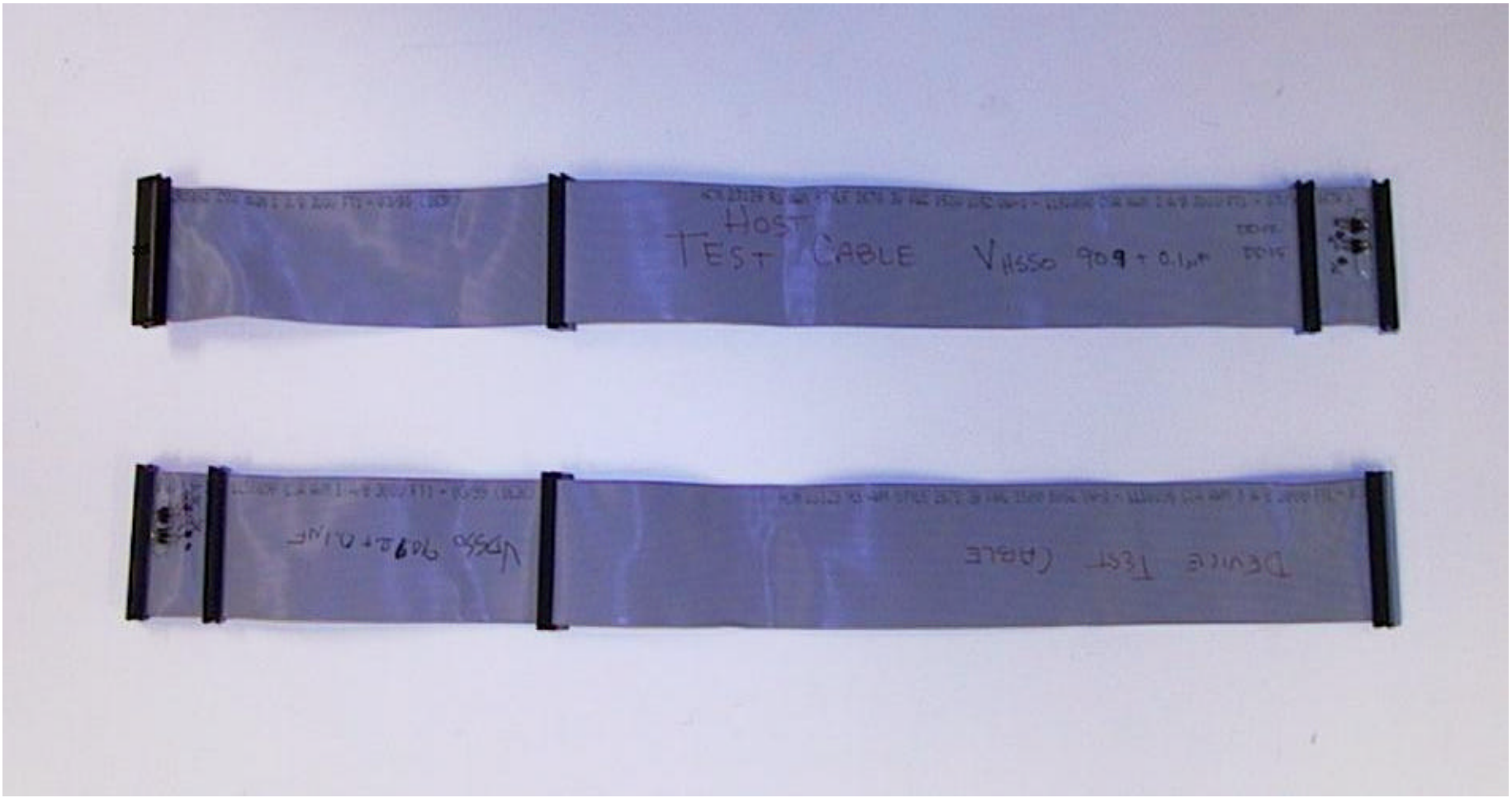


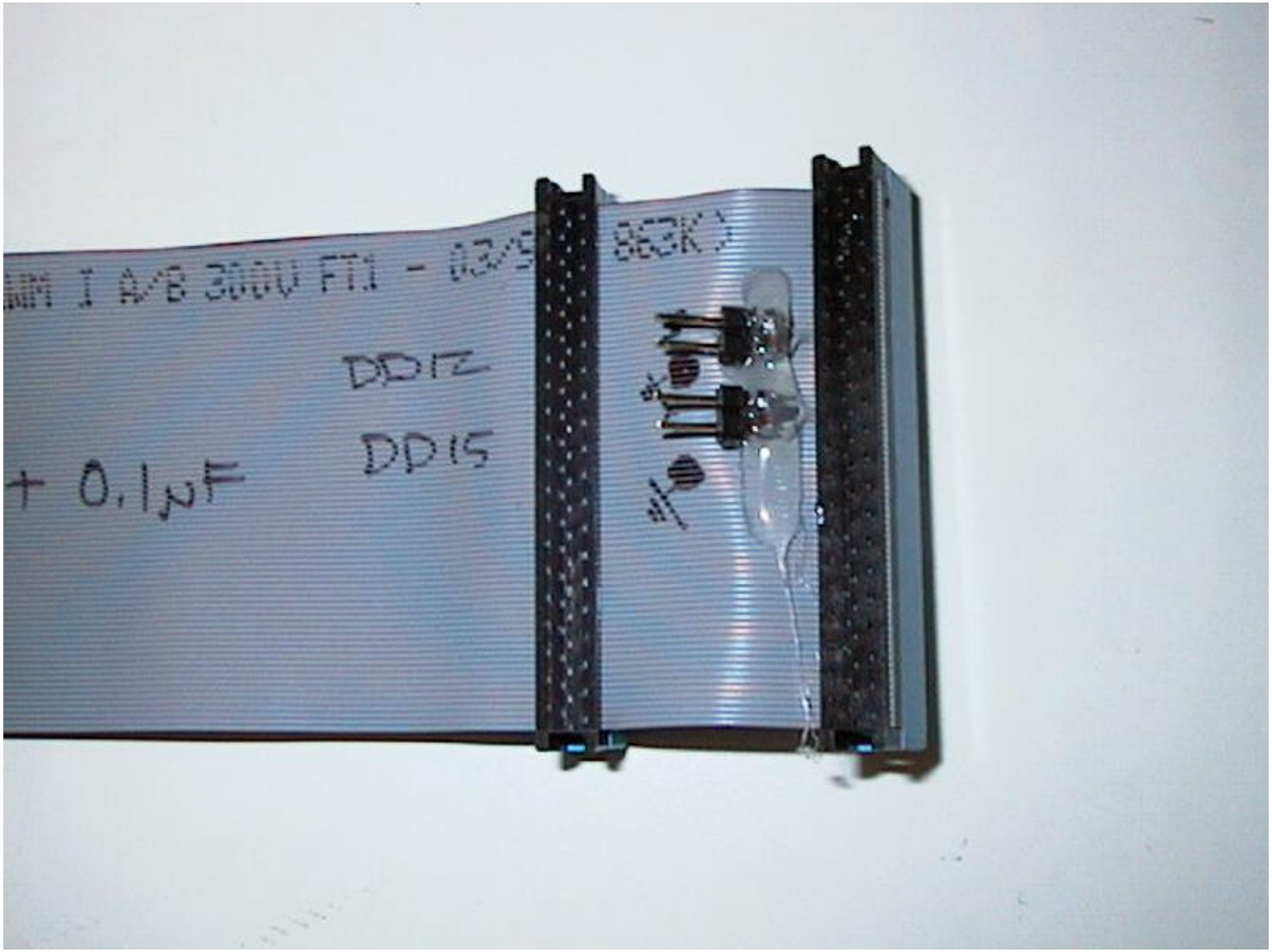
Figure 3: DD12 @ Voh

V_{sso} Test Cable

Desktop
Interface
Engineering



Close-up of Test Point on Test Cable

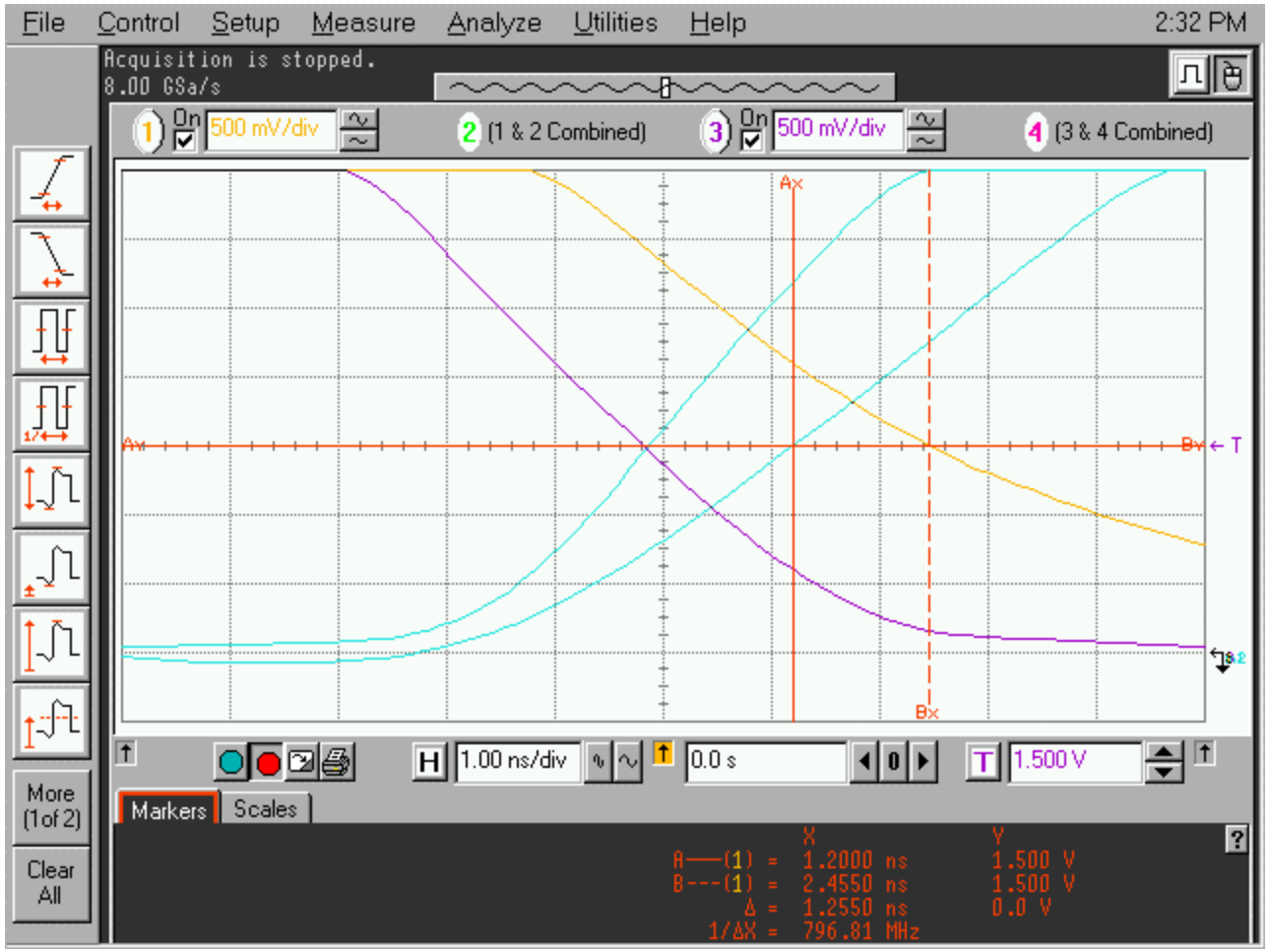


Mode 5 t_{DVS}, t_{DVH}

- **All Ultra DMA modes 0 to 4 may use 5V signaling.**
- **Ultra DMA mode 5 now requires 3.3V signaling.**
- **t_{DVS} and t_{DVH} are measured into a lumped load at the source connector (includes series termination in path).**
  - The skew between a rising and falling edge caused simply by the RC time constant of the series termination and capacitive load is higher with 5V signaling than with 3.3V signaling.
  - Previous simulations showed a maximum of 2.27 ns skew generated through series termination with 5V signaling and capacitive load. This value was mistakenly used to determine t_{DVS} and t_{DVH} for mode 5.
  - New simulations show that with 3.3V signaling, the maximum skew generated through the series termination should be 0.8 ns.
- **If the IC met the IC timing requirement, the system should have already met the mode 5 t_{DVS}, t_{DVH} timings**

Example of source skew with 5V signaling

Desktop Interface Engineering



Example of source skew with 3.3V signaling

Desktop Interface Engineering